



**User Manual**

# MATLAB Toolbox for LPF IS FEE PFM Hardware (Version 2.6)

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**Li Gan, Davor Mance and Peter Zweifel**

Institute of Geophysics
ETH Zürich, Switzerland

# Contents

# List of Abbreviations

| | |
|---|---|
| ADC | Analog-to-Digital Converter |
| AM | Amplitude Modulation |
| ASD | Amplitude Spectral Density |
| AWGN | Additive White Gaussian Noise |
| BP Filter | Band Pass Filter |
| BW | Bandwidth |
| CMD | Command |
| DAC | Digital-to-Analog Converter |
| DMM | Digital Multimeter |
| EL | Electrode |
| ENOB | Effective Number of Bits |
| ESR | Equivalent Series Resistors |
| IS FEE | Inertial Sensor Front End Electronics |
| GRS FEE | Gravity Reference Sensor Front End Electronics |
| FIR | Finite Impulse Response |
| HP Filter | High Pass Filter |
| HR | High Resolution |
| JFET | Junction Gate Field-effect Transistor |
| LISA | Laser Interferometer Space Antenna |
| LP Filter | Low Pass Filter |
| LPF | LISA Pathfinder |
| LSB | Least Significant Bit |
| LTP | LISA Technology Package |
| OpAmp | Operational Amplifier |
| PID | Proportional-Integral-Derivative |

| | |
|---|---|
| PFM | Proto-Flight Model |
| PSD | Power Spectral Density |
| RMS | Root Mean Square |
| SINAD | Signal-to-Noise and Distortion Ratio |
| SNR | Signal-to-Noise Ratio |
| TIA | Transimpedance Amplifier |
| TM | Test Mass |
| WR | Wide Range |

Chapter 1

# Introduction

The *MATLAB Toolbox for LPF IS FEE Hardware* is a collection of MATALB® models for the Inertial Sensor Front End Electronics (IS FEE) hardware in Laser Interferometer Space Antenna (LISA) Pathfinder (LPF). The goal of the modeling is to correctly and accurately represent the functionality and performance of the IS FEE Proto-Flight Model (PFM) hardware in MATLAB. The accuracy of the models can be verified by PFM test results and other requirements of the IS FEE design.

## 1.1. Overview

There are two methods to model the IS FEE PFM hardware in MATALB. The first method is to use Simscape® and Simulink® to build detail models for the hardware, similar like the modeling in Spice softwares. The second method is to describe the hardware in mathematics and then build simplified models using commonly used blocks in Simulink.

Simscape is an extended toolbox in Simulink for modeling systems spanning mechanical, electrical, hydraulic, and other physical domains as physical networks. Its "Foundation Library" provides electrical components, such as resistor, capacitor and inductor etc., which can be used to build user defined electrical network as Spice software. Also, Simscape can generate user defined electrical model by ".ssc" file, which describes the voltage and current relation of the electrical components in the model and can also be used in building user defined electrical network.

In the first modeling method, detail circuit models are constructed using the electrical components provided or generated by Simscape and other components from Simulink. However, due to the high complexity of the models by this method, the simulation is quite slow and not efficient for the simulation of long time period.

In order to improve the simulation speed and thus make the simulation of long time period possible, the second modeling method is considered. In this method, the mathematic models of the hardware are developed by only considering the key electrical components which decide the voltage output performance of the hardware. The circuit current is completely neglected to simplify the models. Therefore, most of the hardware can be represented by their mathematic models which describe the input-output voltage relations, and can be easily built in Simulink using the commonly used blocks. Further simplification can be made by convert-

ing the high frequency operation of the circuit to the equivalent low frequency operation. Therefore, the whole simulation can run in a much lower sampling rate and thus speed up the simulation.

## 1.2. System Requirements and Structure of the Toolbox

The toolbox contains four libraries, i.e., "SSC Library", "Simscape Library", "Simulink Library" and "Simplified Library". The recommended system requirements for the latest version of the toolbox are given in Table 1.1. The toolbox may also work with lower version "MATLAB" and "Simulink Block Library", since only basic functions and blocks are used.

| Software | Version | Request |
|---|---|---|
| MATLAB | 7.11(R2010a) | All libraries |
| Simulink Block Library® | 7.6 | All libraries |
| Signal Processing Blockset® | 7.1 | "Simulink Library" |
| Simscape® | 3.4 | "SSC Library" and "Simscape Library" |
| SimElectronics® | 1.5 | "Simscape Library" |

**Table 1.1** System requirements of the toolbox.

The "SSC Library" contains the models generated by ".ssc" files, and the structure of the library is given below:

```
SSC Library
|-- 6-Port Mutual Inductance
|-- 12-Port Mutual Inductance
```

These models are further used to build transformer models in the "Simscape Library", and the detail of the models including the description of the parameters to set up are introduced in Chapter 2.

The models in "Simscape Library" are classified into two categories: "Foundation Electrical" and "Sensing Hardware". The structure of the library is given below:

```
Simscape Library
|-- Foundation Electronic
    |-- Resistor with Noise
    |-- Three-stage OpAmp
    |-- Three-stage OpAmp (Level 2)
|-- Sensing Hardware
    |-- Transformer
        |-- PFM Transformer (6-Ports Mutual Inductance)
        |-- PFM Transformer (12-Ports Mutual Inductance)
    |-- TIA, JFET Buffer /& Differential Amplifier
        |-- Ideal TIA
        |-- TIA (Three-stage OpAmp + Resistor with Noise)
        |-- JFET Buffer
        |-- Differential Amplifier
    |-- Band Pass Filter
        |-- PFM BP Filter
```

```
    |-- Demodulator
        |-- PFM Demodulator (Ideal)
        |-- PFM Demodulator (Demodulator CMD switch)
|-- @Demo
    |-- @Voltage Divider
    |-- @Differential Amplifier
    |-- @PFM Sensing: Transformer + TIAs
    |-- @PFM Sensing: BP Filter + Demodulator
```

The models in "Foundation Electrical" are used to build the models in "Sensing Hardware". Several demo schemes are provided in "Demo" to demonstrate the functions of the models in the library. Note that the demo of the PFM Sensing is divided into two parts in order to speed up the simulation. The detail of the models in this library including the description of the parameters to set up are introduced in Chapter 2.

**Remark 1**: Some electronic components in "Three-stage OpAmp (Level 2)" and "JFET Buffer" require SimElectronics to be installed in MATLAB. SimElectronics is an extended toolbox in Simscape for modeling and simulating electronic and electromechanical systems, which may need to be purchased in addition. SimElectronics is not required while using other models in "Simscape Library", and also it is not required while using "SSC Library" and "Simulink Library".

The models in the "Simulink Library" are also classified into two categories: "Sensing Hardware" and "Actuation Hardware". The structure of the library is given below:

```
Simunlink Library
|-- Sensing Hardware
    |-- Transformer + TIAs + Diff Amp
    |-- Band Pass Filter
    |-- Demodulator
    |-- ADC (+Noise)
    |-- Transformer + TIAs + Diff Amp for Actuation
    |-- Input Generator
|-- Actuation Hardware
    |-- Waveform Generator (16bit ADC)
    |-- Waveform Generator (24bit ADC)
    |-- AC-DC Splitter
    |-- Attenuator
    |-- PID Controller (16bit ADC)
    |-- PID Controller (24bit ADC)
    |-- Integrator
    |-- ADC
    |-- DAC
    |-- Output Filter
    |-- Output Measurement
    |-- Noise Calculation
|-- @Demo
    |-- @PFM Sensing
    |-- @PFM Actuation (Version 1.0)
    |-- @PFM Actuation (Version 2.0)
    |-- @PFM Actuation Measurement Investigation (Version 1.0)
    |-- @GRS FEE Actuation (20-bit AC DC Parameters, 16-bit ADC)
    |-- @GRS FEE Actuation (20-bit AC DC Parameters, 24-bit ADC)
```

Several demo schemes are provided in "Demo" to demonstrate the functions of the models in the library. The detail of the models in this library including the description of the parameters to set up are introduced in Chapter 3.
**Remark 2**: Some blocks in "Waveform Generator" and "Noise Calculation" require Signal Processing Blockset to be installed in MATLAB.

Based on the models in "Simulink Library", further simplified models are provided in the "Simplified Library". Similarly, the models in this library are classified into two categories: "Sensing Hardware" and "Actuation Hardware". The structure of the library is given below:

```
Simplified Library
|-- Sensing Hardware
    |-- Transformer + TIAs + Diff Amp M-File S-Function
    |-- Transformer + TIAs + Diff Amp C S-Function
    |-- Transformer + TIAs + Diff Amp with Cross Talk M-File S-Function
    |-- Transformer + TIAs + Diff Amp with Cross Talk C S-Function
    |-- Band Pass Filter M-File S-Function
    |-- Band Pass Filter C S-Function
    |-- Demodulator
|-- Actuation Hardware
    |-- Actuation Input EL1 to EL4
    |-- Actuation Input EL5 to EL8
    |-- Actuation Input EL9 to EL12
    |-- Noise Generator (+1/f Noise)
|-- @Demo
    |-- @PFM Sensing (M-File S-Function)
    |-- @PFM Sensing (C S-Function)
    |-- @PFM Sensing Cross Talk (M-File S-Function)
    |-- @PFM Sensing Cross Talk (C S-Function)
    |-- @PFM Actuation Waveform
    |-- @Flicker Noise
```

Several demo schemes are provided in "Demo" to demonstrate the functions of the models in the library. The detail of the models in this library including the description of the parameters to set up are introduced in Chapter 4.

The detail of the demos concerning the sensing and actuation of the PFM hardware are introduced in Chapter 5.

## 1.3. User Guide

The whole toolbox is given in the folder "LISA_IS_FEE_Library", which has the following structure:

```
LISA_IS_FEE_Library
|-- +ssc
    |-- +sscprj
    |-- Six_Port_Mutual_Inductance.ssc
    |-- Twelve_Port_Mutual_Inductance.ssc
|-- +sfun
    |-- +c_sfun
        |-- BP_Filter_CS.c
```

```
        |-- BP_Filter_CS.mexw32
        |-- Transformer_TIAs_DiffAmp_CS.c
        |-- Transformer_TIAs_DiffAmp_CS.mexw32
        |-- Transformer_TIAs_DiffAmp_CT_CS.c
        |-- Transformer_TIAs_DiffAmp_CT_CS.mexw32
    |-- +m_sfun
        |-- ADC_Ref_Noise.m
        |-- BP_Filter_MS.m
        |-- Transformer_TIAs_DiffAmp_CT_MS.m
        |-- Transformer_TIAs_DiffAmp_MS.m
|-- LISA_IS_FEE_Library.mdl
|-- SimplifiedDemo_FlickerNoise.mdl
|-- SimplifiedDemo_IS_FEE_Actuation_Waveform.mdl
|-- SimplifiedDemo_IS_FEE_CrossTalk_CS.mdl
|-- SimplifiedDemo_IS_FEE_CrossTalk_MS.mdl
|-- SimplifiedDemo_IS_FEE_Sensing_CS.mdl
|-- SimplifiedDemo_IS_FEE_Sensing_MS.mdl
|-- SimscapeDemo_DiffAmp.mdl
|-- SimscapeDemo_IS_FEE_Sensing1.mdl
|-- SimscapeDemo_IS_FEE_Sensing2.mdl
|-- SimscapeDemo_VoltageDiv.mdl
|-- SimulinkDemo_GRS_FEE_Actuation_20bit_CMD_16bit_ADC.mdl
|-- SimulinkDemo_GRS_FEE_Actuation_20bit_CMD_24bit_ADC.mdl
|-- SimulInkDemo_IS_FEE_Actuation_MI_v1.mdl
|-- SimulinkDemo_IS_FEE_Actuation_v1.mdl
|-- SimulinkDemo_IS_FEE_Actuation_v2.mdl
|-- SimulinkDemo_IS_FEE_Sensing.mdl
|-- ssc_lib.mdl
```

In order to use this toolbox, the path of the folder must be included in MATLAB. The procedure to include the path of the toolbox in MATLAB is as follows:

1 Copy the toolbox folder to the computer, e.g., in the location of "D:\". Hence, the path of the folder here is "D:\LISA_IS_FEE_Library".

2 Include the path of the toolbox folder in MATALB by clicking "File" → "Set Path ..." → "Add with Subfolders ..." and entering the path of the toolbox folder, i.e., "D:\LISA_IS_FEE_Library" in this example.

Then, by entering "LISA_IS_FEE_Library" in MATLAB command window, the toolbox library will be opened and the models in the library can be used similarly as other Simulink models.

The ".ssc" file of the model in the "SSC Library" can be read by double clicking the block to open the block dialog panel, and then clicking the link "View the source for ..." at the bottom of the model description. The detail of other models can be seen by right clicking the block and selecting "Look Under Mask".

The demos can be run directly by clicking the Start simulation button "▷". Note that proper solver should be chosen for the simulation, i.e., "ode15s(stiff/NDR)" . The solver can be defined in the simulation configuration panel by clicking "Simulation" → "Configuration Parameters ..." on the simulation scheme window. Other simulation parameters, e.g., the end time, can also be set up in this panel.

Chapter 2

# Simscape Models for the Hardware

In this chapter, the models for the "electrical components" are first introduced. The "electrical components" include mutual inductance, resistor with noise and three-stage operational amplifier (OpAmp). The mutual inductance models are generated from ".ssc" file and the other "electrical components" are built using the existing models in Simscape. Then, the models for the PFM sensing hardware are presented, such as transformer, transimpedance amplifier (TIA) and bandpass (BP) filter etc. These models are constructed by the "electrical components" and other models from Simscape and Simulink.

## 2.1. Simscape Models for Electrical Components

### 2.1.1. Mutual inductance

Mutual inductance with two primary coils and one secondary coil is required for modeling the transformer in the sensing hardware, but this type of mutual inductance model is not provided in Simscape library. Thus, the "6-Port Mutual Inductance" with two primary coils and one secondary coil is provided in the "SSC Library". In addition, the "12-Ports Mutual Inductance" is also given in the "SSC Library" in order to provide more precise mutual inductance model for the transformer. In this model, each coil is divided into two so that the inter and intra winding capacitances can be modeled easily.

#### 6-ports mutual inductance

The block diagram of the "6-Ports Mutual Inductance" is shown in Fig. 2.1. The voltages over the primary and secondary coils are given by

$$\begin{aligned} V_1 &= L_1\frac{\mathrm{d}I_1}{\mathrm{d}t} + M_{12}\frac{\mathrm{d}I_2}{\mathrm{d}t} + M_{13}\frac{\mathrm{d}I_3}{\mathrm{d}t} \\ V_2 &= L_2\frac{\mathrm{d}I_2}{\mathrm{d}t} + M_{12}\frac{\mathrm{d}I_1}{\mathrm{d}t} + M_{23}\frac{\mathrm{d}I_3}{\mathrm{d}t} \\ V_3 &= L_3\frac{\mathrm{d}I_3}{\mathrm{d}t} + M_{13}\frac{\mathrm{d}I_1}{\mathrm{d}t} + M_{23}\frac{\mathrm{d}I_2}{\mathrm{d}t} \end{aligned} \tag{2.1}$$

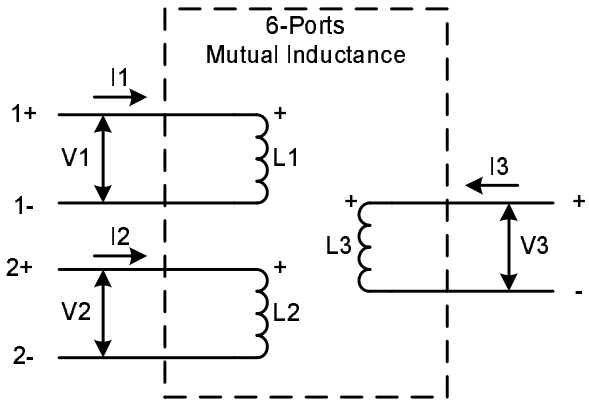


**Figure 2.1** 6-Ports Mutual Inductance.

where $M_{12}$, $M_{13}$ and $M_{23}$ are the mutual inductances defined as

$$\begin{aligned} M_{12} &= k_{12}\sqrt{L_1 L2} \\ M_{13} &= k_{13}\sqrt{L_1 L_3} \\ M_{23} &= k_{23}\sqrt{L_2 L_3}. \end{aligned} \tag{2.2}$$

Here, $k_{12}$, $k_{13}$ and $k_{23}$ are the coupling coefficients. Note that the value of the coupling coefficients must be greater than 0 and less than 1. If the coupling coefficient is equal to 1, there will be simulation problems due to the solver.

The parameters to setup in the model block dialog box are described in Table 2.1.

| **Parameters (Unit)** | **Descriptions** |
|---|---|
| $L_1$, $L_2$, $L_3$ (mH) | Inductances of the coils |
| $k_{12}$, $k_{13}$, $k_{23}$ | Coupling coefficients between the coils |
| $I_{10}$, $I_{20}$, $I_{30}$ (A) | Initial currents of the coils $L_1$, $L_2$, $L_3$ |

**Table 2.1** Parameters to setup in "6-Ports Mutual Inductance".

### 12-ports mutual inductance

The block diagram of "12-Ports Mutual Inductance" is shown in Fig. 2.2. The voltage over the coil $i$ is

$$V_i = L_i \frac{\mathrm{d}I_i}{\mathrm{d}t} + \sum_{j \neq i} M_{ij} \frac{\mathrm{d}I_j}{\mathrm{d}t}, \quad 1 \leq i \neq j \leq 6 \tag{2.3}$$

where $M_{ij}$ is the mutual inductance between coils $i$ and $j$, defined as

$$M_{ij} = k_{ij}\sqrt{L_i L_j}, \quad 1 \leq i \neq j \leq 6. \tag{2.4}$$

Here, $k_{ij}$ is the coupling coefficient between the coil $i$ and $j$. Note that the value of the coupling coefficients must be greater than 0 and less than 1. If the coupling coefficient is equal to 1, there will be simulation problems due to the solver.

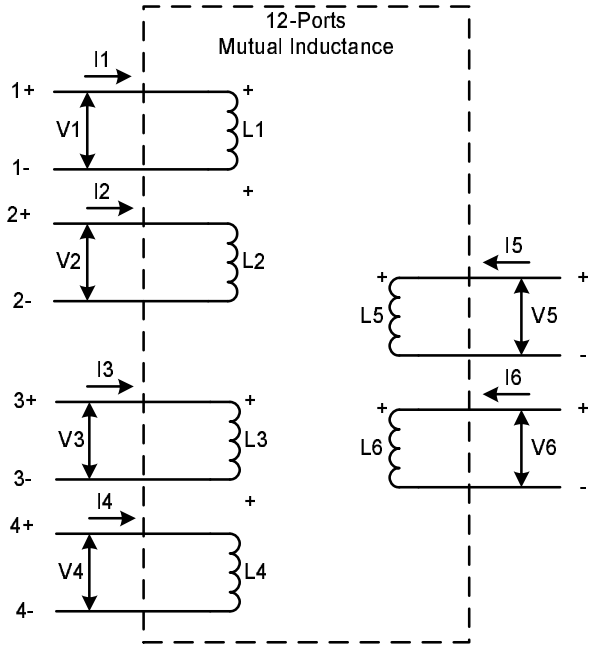


**Figure 2.2** 12-Ports Mutual Inductance.

| **Parameters (Unit)** | **Descriptions** |
|---|---|
| $L_1$ to $L_6$ (mH) | Inductances of the coils |
| $k_{12}$ to $k_{56}$ | Coupling coefficients between the coils |

**Table 2.2** Parameters to setup in "12-Ports Mutual Inductance".

The parameters to setup in the model block dialog box are described in Table 2.2.

### 2.1.2. Resistor with noise

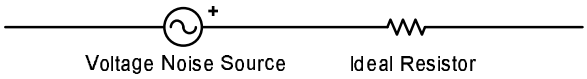


**Figure 2.3** "Resistor with Noise" simplified circuit model.

Since there is only ideal resistor model in Simscape, the "Resistor with Noise" model is built in order to provide practical resistor model with thermal noise. The "Resistor with Noise" model can be constructed as an ideal resistor connected in series with a voltage noise source or in parallel with a current noise source [1]. Here, we model it as an ideal resistor connected in series with a voltage noise source, as shown in Fig. 2.3.

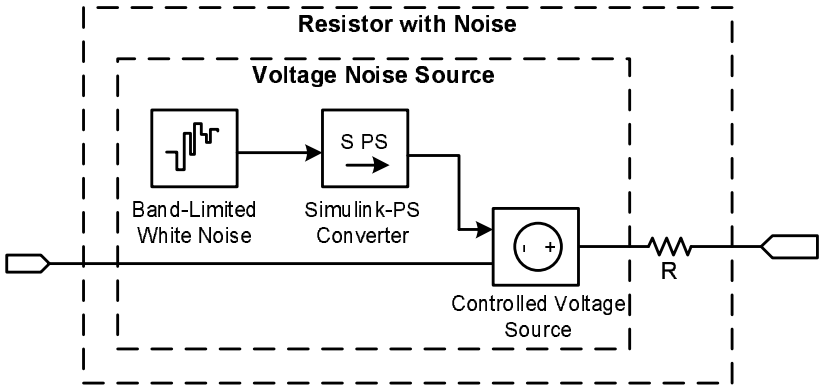


**Figure 2.4** Simscape model: "Resistor with Noise".

The "Resistor with Noise" model in Simscape is given in Fig. 2.4. The ideal resistor comes from the "Foundation Library\Electrical\Electrical Elements" in Simscape, and the voltage noise source is constructed as follows: A band-limited additive white Gaussian noise (AWGN) is generated by the Simulink block "Band-Limited White Noise". In order to communicate with other Simscape models, the output of the "Band-Limited White Noise" block is converted to physical signal by the "Simulin-PS Converter". Then, this physical signal is used to control the "Controlled Voltage Source" in order to generate the voltage output of the noise source. The noise sources in the later sections are also built using this method. The "Simulin-PS Converter" and "Controlled Voltage Source" can be found in the "Utilities" and "Foundation Library\Electrical\Electrical Sources" in Simscape, respectively.

In general, the noise power of the resistor is defined as [1]

$$P_r = \int_{f_h}^{f_l} 4K_bTR\mathrm{d}f = 4K_bTR(f_h - f_j) \tag{2.5}$$

where $K_b$ is the Boltzmann's constant equal to $1.38 \times 10^{-23} J/K$, $T$ is the temperature in Kelvin, $R$ is the resistance value in Ohm, $f_h$ and $f_l$ are the highest and lowest operation frequency, respectively. Here, the power of the "Band-Limited White Noise" block is defined as

$$\tilde{P}_r = P_r \times T_s \tag{2.6}$$

in order to produce correct noise power level for the block, where $T_s$ is the sampling time.

The parameters to setup in the model block dialog box are described in Table 2.3. Note that the voltage noise source can be switched on or off, which is not shown in Fig. 2.4.

| **Parameters (Unit)** | **Descriptions** |
|---|---|
| $R$ (Ohm) | Resistance |
| $T$ (Kelvin) | Temperature |
| $f_h$, $f_l$ (Hz) | Highest and lowest operation frequency |
| $T_s$ (s) | Sampling time |
| Resistor Noise Switch (1:On, 0:OFF) | Switch on or off the voltage noise source |

**Table 2.3** Parameters to setup in "Resistor with Noise".

### 2.1.3. Three-stage operational amplifier

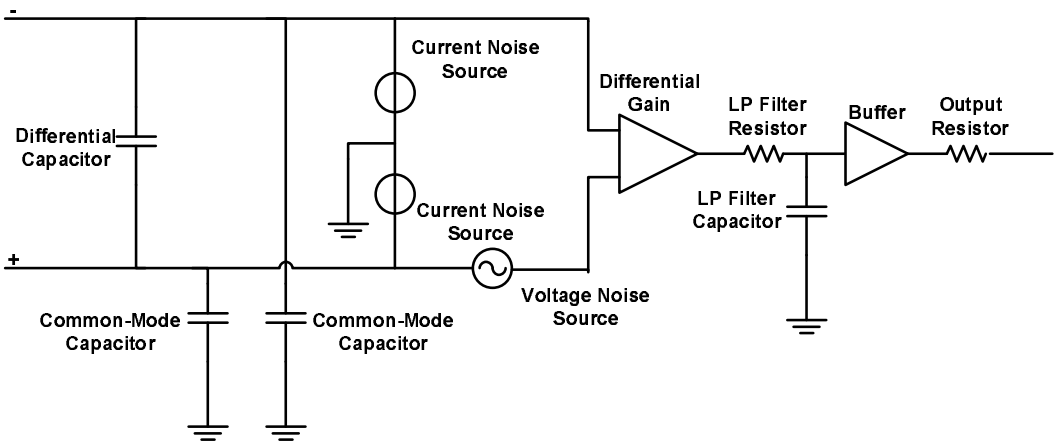


**Figure 2.5** "Three-stage OpAmp" simplified circuit model.

Since there is only ideal OpAmp model in Simscape, the "Three-stage OpAmp" model is built in order to provide more realistic OpAmp model with input capacitance, voltage and current noise sources etc. The three stages are the input stage – differential amplifier stage, the middle stage – gain\frequency response stage, and the output stage – output buffer stage, as shown in Fig. 2.5. The differential amplifier stage includes the input resistor, common-mode capacitor, differential capacitor, voltage noise source, current noise source and differential voltage gain. The noise source models in OpAmp are introduced in [1]. The gain\frequency response stage is modeled as a passive RC low pass (LP) filter, in order to limit the operating bandwidth. The output buffer stage contains the voltage buffer and output resistor.

The "Three-stage OpAmp" model in Simscape is given in Fig. 2.6. The "capacitor" comes from the "Foundation Library\Electrical\Electrical Elements" in Simscape. The current and voltage noise sources are constructed similarly as the voltage noise source in Section 2.1.2. The differential voltage gain is modeled using "Voltage-Controlled Voltage Source" with the value equal to the open loop gain of the OpAmp. The buffer in the output stage is also modeled using "Voltage-Controlled Voltage Source" with unity gain. The "Voltage-Controlled Voltage Source" can be found in "Foundation Library\Electrical\Electrical Sources" in Simscape.

In general, the powers of the voltage and current noise sources are defined as

$$\begin{aligned} P_v &= S_v^2(f_h - f_l) \\ P_i &= S_i^2(f_h - f_l) \end{aligned} \tag{2.7}$$

where $S_v$ and $S_i$ are the voltage noise density and current noise density, respectively, $f_h$ and $f_l$ are the highest and lowest operation frequency, respectively. Here, the powers of the "Band-Limited White Noise" blocks for the voltage and current noise sources are defined as

$$\begin{aligned} \tilde{P}_v &= P_v \times T_s \\ \tilde{P}_i &= P_i \times T_s \end{aligned} \tag{2.8}$$

in order to produce correct noise power level for the block, where $T_s$ is the sampling time.

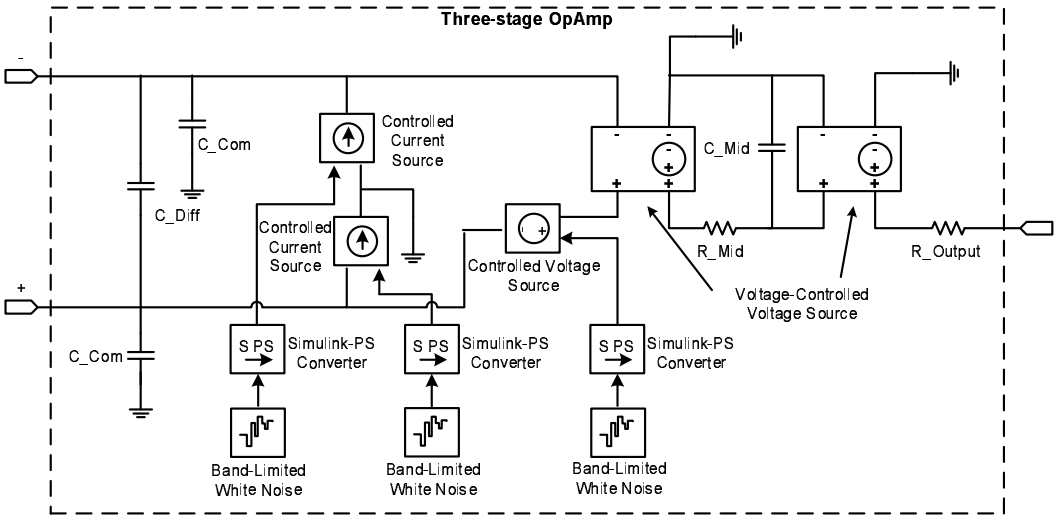


**Figure 2.6** Simscape model: "Three-stage OpAmp".

The parameters to setup in the model block dialog box are described in Table 2.4. Normally, these parameters can be found in the data sheet of the OpAmp. Note that the noise sources can be switched on or off, which is not shown in Fig. 2.6.

| Panels | Parameters (Unit) | Descriptions |
|---|---|---|
| Input Stage | $C_{Com}$ (pF) | Common mode capacitance |
| | $C_{Diff}$ (pF) | Differential capacitance |
| | $S_v$ (V/sqrt(Hz)) | Voltage noise density |
| | $S_i$ (A/sqrt(Hz)) | Current noise density |
| | Open Loop Gain (dB) | Open loop gain of the OpAmp |
| | Input Noise Switch (1:On, 0:OFF) | Switch on or off the noise sources |
| Middle and Output Stages | $R_{Mid}$ (Ohm) | LP filter resistance |
| | $C_{Mid}$ (F) | LP filter capacitance |
| | $R_{Output}$ (Ohm) | Output resistance |
| Others | $f_h$, $f_l$ (Hz) | Highest and lowest operation frequency |
| | $T_s$ (s) | Sampling time |

**Table 2.4** Parameters to setup in "Three-stage OpAmp".

### 2.1.4. Three-stage operational amplifier (Level 2)

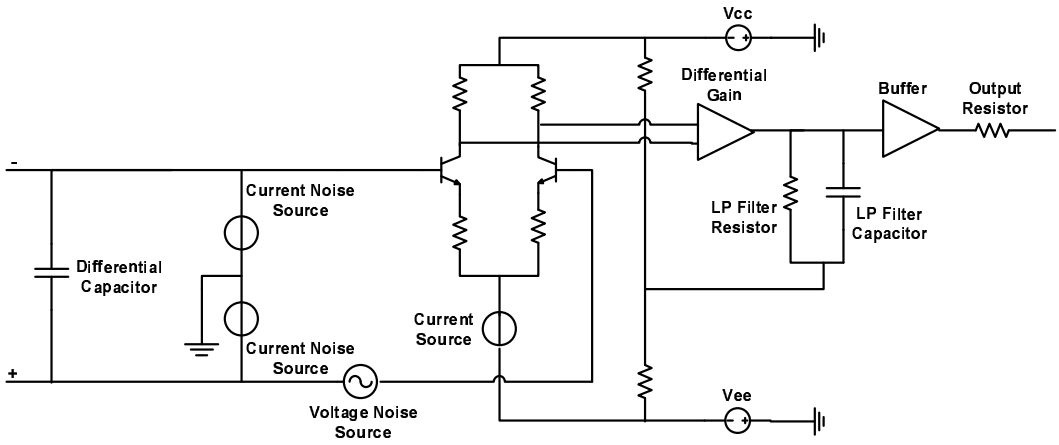


**Figure 2.7** "Three-stage OpAmp (Level 2)" simplified circuit model.

The level 2 three-stage operational amplifier is also provided in the library. In this model, the differential amplifier is modeled by bipolar transistors, and the internal voltage reference is also included, as shown in Fig. 2.7. Here, the common mode capacitors in the input stage are neglected to simplify the model.

The "Three-stage OpAmp (Level 2)" model in Simscape is given in Fig. 2.8. The "capacitor" comes from the "Foundation Library\Electrical\Electrical Elements" in Simscape. The current and voltage noise sources are constructed similarly as the voltage noise source in Section 2.1.2. The NPN bipolar transistor comes from the "SimElectronics\Semiconductor Devices". The differential voltage gain is modeled using "Voltage-Controlled Voltage Source", and the buffer in the output stage is also modeled using "Voltage-Controlled Voltage Source" with unity gain. The "Voltage-Controlled Voltage Source" can be found in "Foundation Library\Electrical\Electrical Sources" in Simscape. The powers of the voltage and current noise sources are defined similarly as in Section 2.1.3 with

$$\begin{aligned} \tilde{P}_v &= P_v \times T_s = S_v^2(f_h - f_l)T_s \\ \tilde{P}_i &= P_i \times T_s = S_i^2(f_h - f_l)T_s. \end{aligned} \tag{2.9}$$

The parameters to setup in the model block dialog box are described in Table 2.5. Normally, these parameters can be found in the data sheet of the OpAmp. Note that the voltage noise source can be switched on or off, which is not shown in Fig. 2.8.

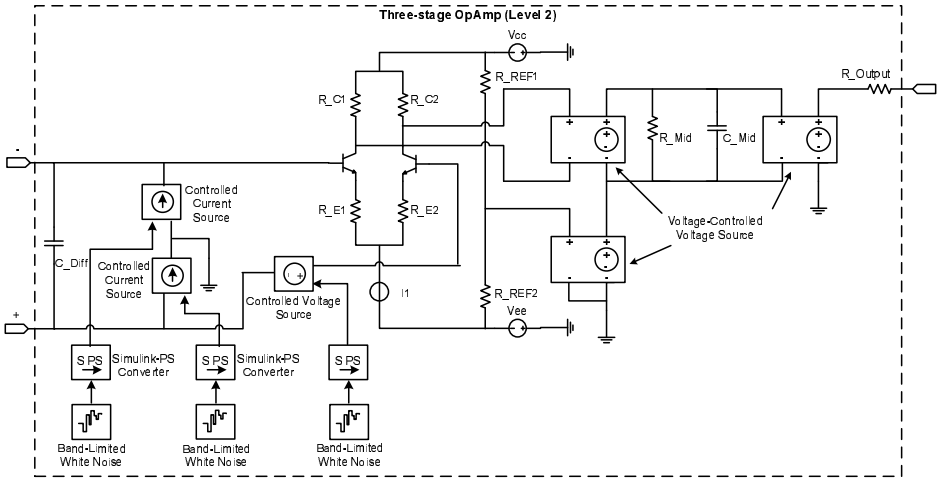


**Figure 2.8** Simscape model: "Three-stage OpAmp (Level 2)".

| Panels | Parameters (Unit) | Descriptions |
|---|---|---|
| Input Stage | $C_{Diff}$ (pF) | Differential capacitance |
| | $S_v$ (V/sqrt(Hz)) | Voltage noise density |
| | $S_i$ (A/sqrt(Hz)) | Current noise density |
| | Voltage Gain (S) | Voltage gain |
| | $I1$ (A) | Differential amplifier bias current |
| | BJT Forward Current Transfer Ratio | BJT Parameters |
| | $R_{C1}$, $R_{C2}$ (Ohm) | Collector resistance |
| | $R_{E1}$, $R_{E2}$ (Ohm) | Emitter resistance |
| | Input Noise Switch (1:On, 0:OFF) | Switch on or off the noise sources |
| Middle and Output Stages | $R_{Mid}$ (Ohm) | LP filter resistance |
| | $C_{Mid}$ (F) | LP filter capacitance |
| | $R_{Output}$ (Ohm) | Output resistance |
| Others | Vcc, Vee (V) | Supply Voltage VCC, VEE |
| | $f_h$, $f_l$ (Hz) | Highest and lowest operation frequency |
| | $T$ (Kelvin) | Temperature |
| | $T_s$ (s) | Sampling time |

**Table 2.5** Parameters to setup in "Three-stage OpAmp (Level 2)".

## 2.2. Simscape Models for IS FEE PFM Sensing Hardware

The schematics and layouts of the IS FEE sensing hardware are given in [2], where the circuits of the TIA, JFET buffer, differential amplifier, BP filter and demodulator are defined.

### 2.2.1. Transformer

Two transformer models, which are "PFM Transformer (6-Ports Mutual Inductance)" and "PFM Transformer (12-Ports Mutual Inductance)", are provided in the "Simscape Library".

#### PFM transformer (6-ports mutual inductance)

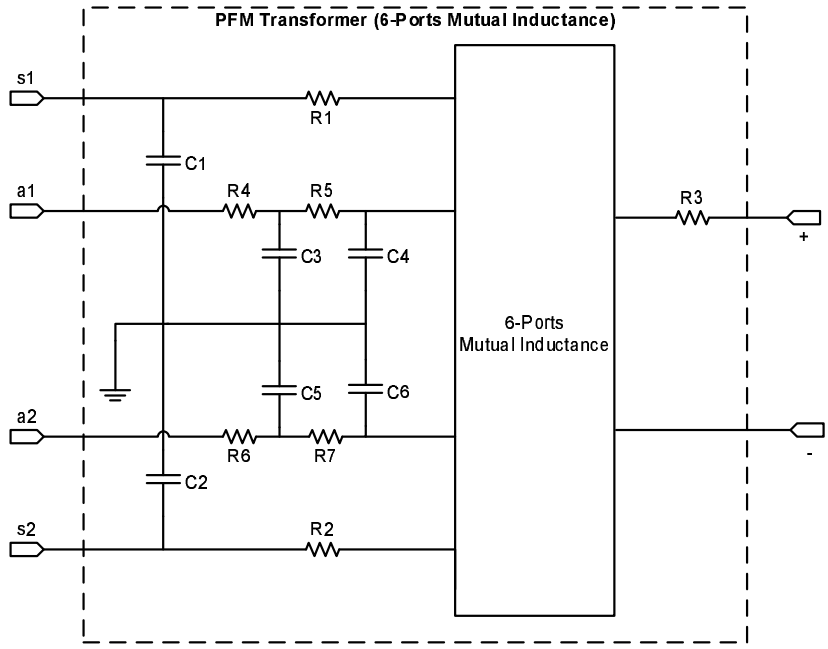


**Figure 2.9** Simscape model: "PFM Transformer (6-Ports Mutual Inductance)".

The "PFM Transformer (6-Ports Mutual Inductance)" is constructed by the "6-Ports Mutual Inductance" in the "SSC Library", the "Resistor with Noise" in Section 2.1.2 and the "capacitor" from the "Foundation Library\Electrical\Electrical Elements" in Simscape. The circuit model is investigated using MicroCap® in [3] and the Simscape model is given in Fig. 2.9, where "s1" and "s2" are the sensing input ports, and "a1" and "a2" are the actuation input ports.

The parameters to setup in the model block dialog box are described in Table 2.6. The approximated values of each parameter for the PFM hardware are also given in the table. Here, "$K_{12}$", "$K_{13}$" and "$K_{23}$" represent the "Primary - Primary Coupling Coefficient", "Upper Primary - Secondary Coupling Coefficient" and "Lower Primary - Secondary Coupling Coefficient", respectively.

| Panels | Parameters (Unit) | Descriptions (Values) |
|---|---|---|
| Primary arms (upper and lower) | $L_1$, $L_2$ (mH) | Coil inductances (4.2) |
| | $R_1$, $R_2$ (Ohm) | Coil resistance (4) |
| | $C_1$, $C_2$ (pF) | Input capacitance (300) |
| Secondary Arm | $L_3$ (mH) | Coil inductances (4.2) |
| | $R_3$ (Ohm) | Coil resistance (4) |
| Actuation Circuit | $R_4$ to $R_7$ (Ohm) | LP filter resistance ($3.3 \times 10^3$) |
| | $C_3$ to $C_6$ (nF) | LP filter capacitance (10) |
| Others | $K_{12}$, $K_{13}$, $K_{23}$ | Coupling coefficients (0.99) |
| | $f_h$, $f_l$ (Hz) | Highest and lowest operation frequency ($10^6$,1) |
| | $T$ (Kelvin) | Temperature (300) |
| | $T_s$ (s) | Sampling time ($1/(2 \times 10^6)$) |
| | Noise Switch (1:On, 0:OFF) | Switch on or off the resistor noise |

**Table 2.6** Parameters to setup in "PFM Transformer (6-Ports Mutual Inductance)".

### PFM transformer (12-ports mutual inductance)

The "PFM Transformer (12-Ports Mutual Inductance)" is constructed by the "12-Ports Mutual Inductance" in the "SSC Library", the "Resistor with Noise" in Section 2.1.2 and the "capacitor" from the "Foundation Library\Electrical\Electrical Elements" in Simscape. The circuit model is investigated using MicroCap in [4] and the Simscape model is given in Fig. 2.10, where "s1" and "s2" are the sensing input ports, and "a1" and "a2" are the actuation input ports.

The parameters to setup in the model block dialog box are described in Table 2.7. The approximated values of each parameter for the PFM hardware are also given in the table. Here, "$K_{PP}$", "$K_{P1S}$", "$K_{P2S}$" and "$K_{SS}$" represent the "Primary - Primary Coupling Coefficient", "Upper Primary - Secondary Coupling Coefficient", "Lower Primary - Secondary Coupling Coefficient" and "Secondary - Secondary Coupling Coefficient", respectively.

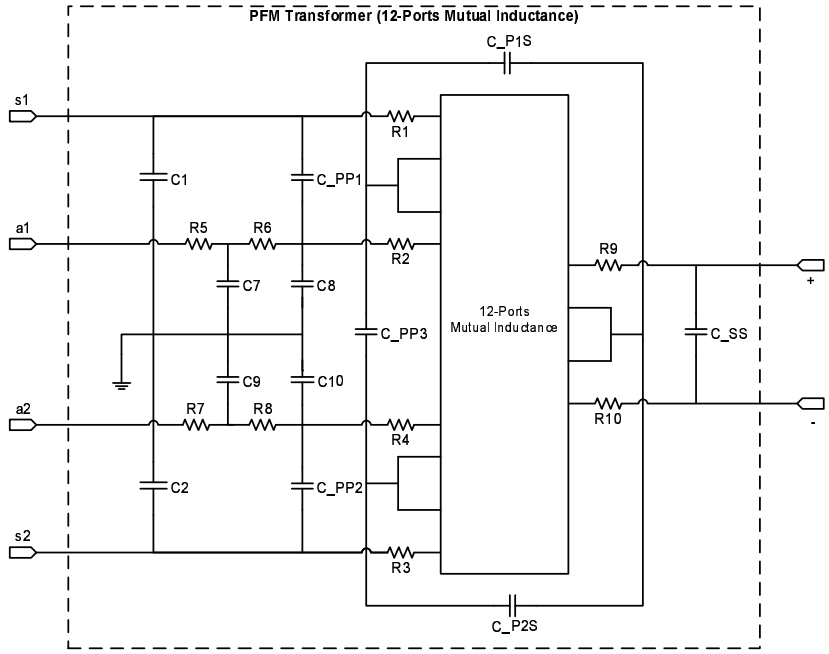


**Figure 2.10** Simscape model: "PFM Transformer (12-Ports Mutual Inductance)".

| **Panels** | **Parameters (Unit)** | **Descriptions (Values)** |
|---|---|---|
| Primary Arms (upper and lower) | $L_1$ to $L_4$ (mH) | Coil inductances (0.975) |
| | $R_1$ to $R_4$ (Ohm) | Coil resistance (8) |
| | $C_{PP1}$ to $C_{PP3}$ (pF) | Intra winding capacitance (10) |
| | $C_{P1S}$, $C_{P2S}$ (pF) | Inter winding capacitance (10) |
| | $C_1$, $C_2$ (pF) | Input capacitance (300) |
| Secondary Arm | $L_5$, $L_6$ (mH) | Coil inductances (0.975) |
| | $R_9$, $R_{10}$ (Ohm) | Coil resistance (10) |
| | $C_{SS}$ (pF) | Intra winding capacitance (10) |
| Actuation Circuit | $R_5$ to $R_8$ (Ohm) | LP filter resistance ($3.3 \times 10^3$) |
| | $C_7$ to $C_{10}$ (nF) | LP filter capacitance (10) |
| Others | $K_{PP}$, $K_{P1S}$, $K_{P2S}$, $K_{SS}$ | Coupling coefficients (0.99) |
| | $f_h$, $f_l$ (Hz) | Highest and lowest operation frequency ($10^6$, 1) |
| | $T$ (Kelvin) | Temperature (300) |
| | $T_s$ (s) | Sampling time ($1/(2 \times 10^6)$) |
| | Noise Switch (1:On, 0:OFF) | Switch on or off the resistor noise |

**Table 2.7** Parameters to setup in "PFM Transformer (12-Ports Mutual Inductance)".

### 2.2.2. TIA

Two TIA models, which are the "Ideal TIA" and "TIA (Three-stage OpAmp + Resistor with Noise)", are provided in the "Simscape Library".

#### Ideal TIA

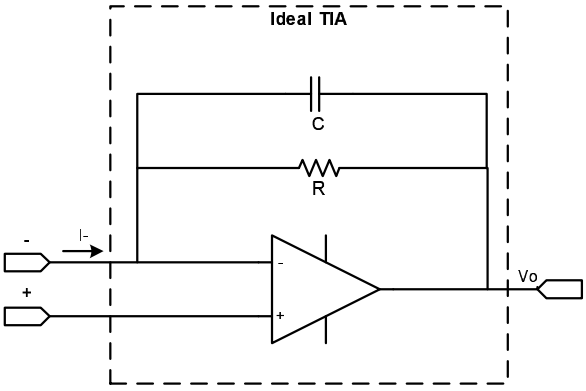


**Figure 2.11** Simscape model: "Ideal TIA".

The "Ideal TIA" is constructed by the "ideal OpAmp", "resistor" and "capacitor" models from the "Foundation Library\Electrical\Electrical Elements" in Simscape. The Simscape model is given in Fig. 2.11, where "+" and "-" denote the input ports connected to the positive and negative inputs of the OpAmp, respectively.

The parameters to setup in the model block dialog box are described in Table 2.8. The values of the feedback resistor and capacitor for the PFM hardware are also given in the table.

| Parameters (Unit) | Descriptions (Values) |
|---|---|
| $R$ (Ohm) | Feedback resistance ($5.6 \times 10^{6}$) |
| $C$ (F) | Feedback capacitance ($3.3 \times 10^{-12}$) |

**Table 2.8** Parameters to setup in "Ideal TIA".

#### TIA (Three-stage OpAmp + Resistor with Noise)

The "TIA (Three-stage OpAmp + Resistor with Noise)" is constructed by the "Three-stage OpAmp" in Section 2.1.3, the "Resistor with Noise" in Section 2.1.2 and the "capacitor" from the "Foundation Library\Electrical\Electrical Elements" in Simscape. The Simscape model is given in Fig. 2.12, where "+" and "-" denote the input ports connected to the positive and negative inputs of the OpAmp, respectively.

The parameters to setup in the model block dialog box are described in Table 2.9. The values of each parameter for the PFM hardware are also given in the table. Note that the OpAmp used in the sensing hardware is "OP467" from Analog Devices®, and the parameters of the OpAmp are defined in [5].

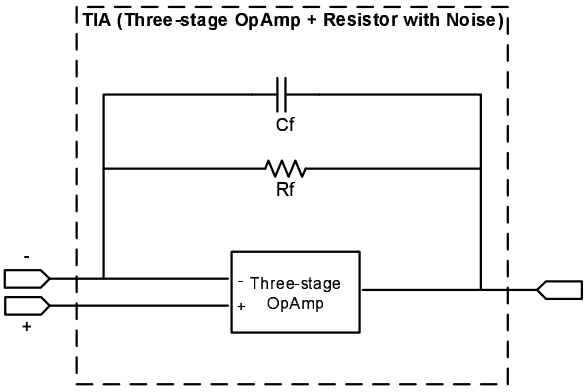


**Figure 2.12** Simscape model: "TIA (Three-stage OpAmp + Resistor with Noise)".

| Panels | Parameters (Unit) | Descriptions (Values) |
|---|---|---|
| Input Stage (OpAmp) | $C_{Com}$ (pF) | Common mode capacitance (2) |
| | $C_{Diff}$ (pF) | Differential capacitance (1) |
| | $S_v$ (V/sqrt(Hz)) | Voltage noise density ($6 \times 10^{-9}$) |
| | $S_i$ (A/sqrt(Hz)) | Current noise density ($0.8 \times 10^{-12}$) |
| | Open Loop Gain (dB) | Open loop gain of the OpAmp (80) |
| | Input Noise Switch (1:On, 0:OFF) | Switch on or off the OpAmp noise sources |
| Middle and Output Stages (OpAmp) | $R_{Mid}$ (Ohm) | LP filter resistance ($10^5$) |
| | $C_{Mid}$ (F) | LP filter capacitance ($3.98 \times 10^{-10}$) |
| | $R_{Output}$ (Ohm) | Output resistance (55) |
| Feedback | $R_f$ (Ohm) | Feedback resistance ($5.6 \times 10^6$) |
| | $C_f$ (pF) | Feedback capacitance (3.3) |
| | Resistor Noise Switch (1:On, 0:OFF) | Switch on or off the resistor noise |
| Others | $f_h$, $f_l$ (Hz) | Highest and lowest operation frequency ($10^6$) |
| | $T$ (Kelvin) | Temperature (300) |
| | $T_s$ (s) | Sampling time ($1/(2 \times 10^6)$) |

**Table 2.9** Parameters to setup in "TIA (Three-stage OpAmp + Resistor with Noise)".

### Theory

Assuming the positive input of the OpAmp is connected to the ground, the voltage output of the "Ideal TIA" $V_o$ becomes

$$V_o = \frac{R}{1 + sRC} I_- \tag{2.10}$$

where $s = j\omega$, $R$ is the feedback resistance, $C$ is the feedback capacitance and $I_-$ is the current into the input port "-". Thus, the TIA converts the current input to voltage output via the negative feedback of the OpAmp. Since the OpAmp model in "TIA (Three-stage OpAmp + Resistor with Noise)" is not ideal, the voltage output of the TIA will be affected by the parameters of the OpAmp, e.g., the input capacitance and the open loop gain.

### 2.2.3. JFET buffer

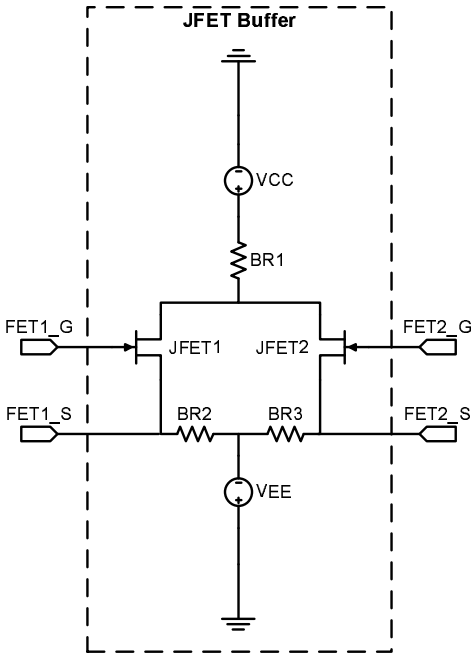


**Figure 2.13** Simscape model: "JFET Buffer".

The "JFET Buffer" is constructed by the "N-Channel JFET" from the "SimElectronics\Semiconductor Devices" and the "resistor" from the "Foundation Library\Electrical\Electrical Elements" in Simscape. The Simscape model is given in Fig. 2.13. The JFET buffer is used to reduce the input capacitance of the OpAmp [6] and the performance is investigated in [4].

The parameters to setup in the model block dialog box are described in Table 2.10. The resistor values of the buffer circuit for the PFM hardware are also given in the table. Note that the JFET used in the sensing hardware is "2N4393" [7] from Linear System®.

| **Panels** | **Parameters (Unit)** | **Descriptions (Values)** |
|---|---|---|
| Ohmic Resistance | $R_s$ (Ohm) | Source Ohmic Resistance |
| (JFET) | $R_d$ (Ohm) | Drain Ohmic Resistance |
| Junction Capacitance | $C_{gs}$ (pF) | Gate-source capacitance |
| (JFET) | $C_{gd}$ (F) | Gate-drain capacitance |
| Buffer Circuit | $BR_1$ (Ohm) | Resistance ($10^3$) |
| | $BR_2$, $BR_3$ (Ohm) | Resistance ($32.4 \times 10^3$) |
| | Vcc, Vee (V) | Supply voltage VCC (13), VEE ($-5$) |
| | Resistor Noise Switch (1:On, 0:OFF) | Switch on or off the resistor noise |
| Others | $f_h$, $f_l$ (Hz) | Highest and lowest operation frequency ($10^6$, 1) |
| | $T$ (Kelvin) | Temperature (300) |
| | $T_s$ (s) | Sampling time ($1/(2 \times 10^6)$) |

**Table 2.10** Parameters to setup in "JFET Buffer".

### 2.2.4. Differential amplifier

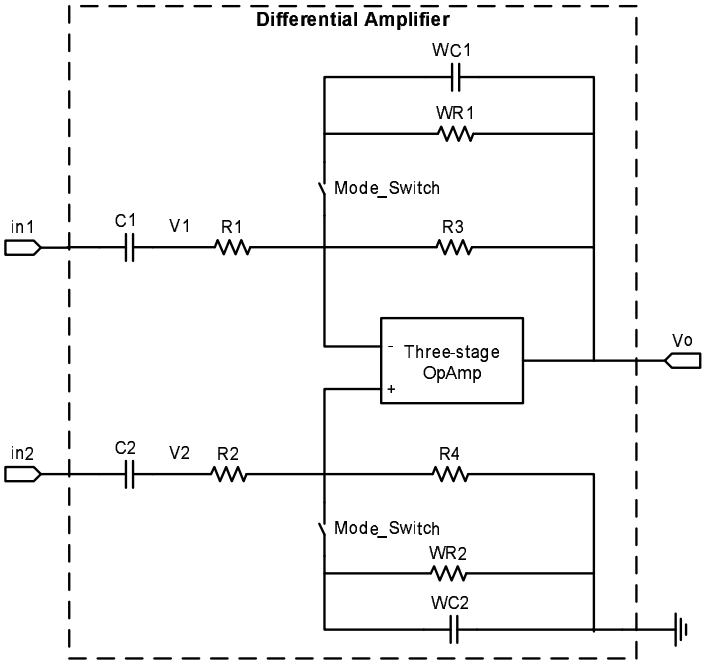


**Figure 2.14** Simscape model: "Differential Amplifier".

The "Differential Amplifier" is constructed by the "Three-stage OpAmp" in Section 2.1.3, the "Resistor with Noise" in Section 2.1.2 and the "capacitor" from the "Foundation Library\Electrical\Electrical Elements" in Simscape. The Simscape model is given in Fig. 2.14, where "in1" and "in2" are the two input ports of the differential amplifier.

The parameters to setup in the model block dialog box are described in Table 2.11. The values of each parameter for the PFM hardware are also given in the table. Note that the OpAmp used in the sensing hardware is "OP467" [5].

#### Theory

Assuming the OpAmp in the differential amplifier is ideal and neglecting the decoupling capacitors at the input, the voltage output of the differential amplifier $V_o$ at high resolution (HR) mode is (*cf.* Fig. 2.14)

$$V_o = \left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R1}\right)V_2 - \frac{R_3}{R_1}V_1. \tag{2.11}$$

where $V_1$ and $V_2$ are the input voltages. Assuming that the resistors are chosen as $R_1 = R_2$ and $R_3 = R_4$, (2.11) becomes

$$V_o = \frac{R_3}{R_1}(V_2 - V_1). \tag{2.12}$$

In wide range (WR) model, similar results can be produced by considering the WR model capacitor and resistor.

| **Panels** | **Parameters (Unit)** | **Descriptions (Values)** |
|---|---|---|
| Input Stage (OpAmp) | $C_{Com}$ (pF) | Common mode capacitance (2) |
| | $C_{Diff}$ (pF) | Differential capacitance (1) |
| | $S_v$ (V/sqrt(Hz)) | Voltage noise density ($6 \times 10^{-9}$) |
| | $S_i$ (A/sqrt(Hz)) | Current noise density ($0.8 \times 10^{-12}$) |
| | Open Loop Gain (dB) | Open loop gain of the OpAmp (80) |
| | Input Noise Switch (1:On, 0:OFF) | Switch on or off the OpAmp noise sources |
| Middle and Output Stages (OpAmp) | $R_{Mid}$ (Ohm) | LP filter resistance ($10^5$) |
| | $C_{Mid}$ (F) | LP filter capacitance ($3.98 \times 10^{-10}$) |
| | $R_{Output}$ (Ohm) | Output resistance (55) |
| Differential Amplifier Circuit | $C_1$, $C_2$ (nF) | Decoupling capacitance (10) |
| | $R_1$, $R_2$ (Ohm) | HR mode resistance (976) |
| | $R_3$, $R_4$ (Ohm) | HR mode resistance ($18.7 \times 10^3$) |
| | $WC_1$, $WC_2$ (pF) | WR model capacitance (100) |
| | $WR_1$, $WR_2$ | WR model resistance (909) |
| | Resistor Noise Switch (1:On, 0:OFF) | Switch on or off the resistor noise |
| Others | Mode Switch (1:On, 0:OFF) | Switch to HR or WR mode |
| | $R_{Switch}$ (Ohm) | Switch close resistance (35) |
| | $G_{Switch}$ (S) | Switch open conductance ($10^{-13}$) |
| | $f_h$, $f_l$ (Hz) | Highest and lowest operation frequency ($10^6$, 1) |
| | $T$ (Kelvin) | Temperature (300) |
| | $T_s$ (s) | Sampling time ($1/(2 \times 10^6)$) |

**Table 2.11** Parameters to setup in "Differential Amplifier".

### 2.2.5. Bandpass filter

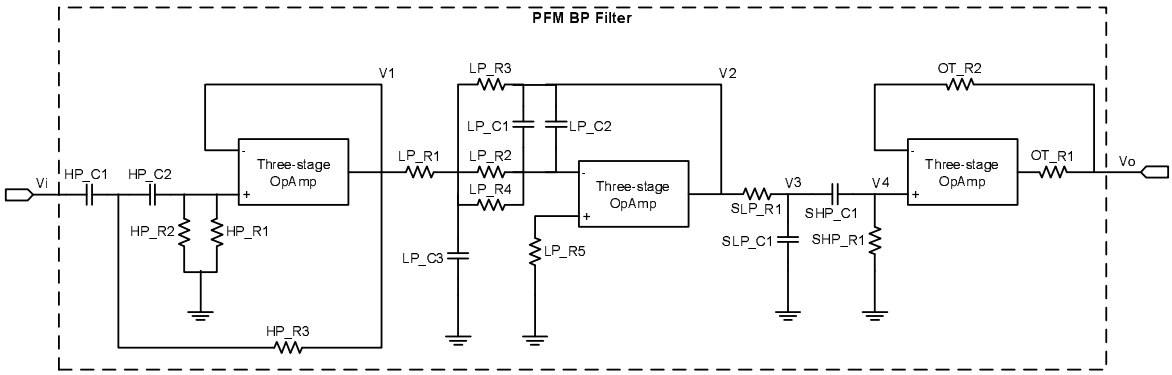


**Figure 2.15** Simscape model: "PFM BP Filter".

The "PFM BP Filter" is constructed by the "Three-stage OpAmp" in Section 2.1.3, the "Resistor with Noise" in Section 2.1.2 and the "capacitor" from the "Foundation Library\Electrical\Electrical Elements" in Simscape. The Simscape model is given in Fig. 2.15.

The parameters to setup in the model block dialog box are described in Table 2.12. The valuess of each parameter for the PFM hardware are also given in the table. Note that the OpAmp used in the sensing hardware is "OP467" [5].

#### Theory

Here we assume that the OpAmp is ideal and notice that the high pass (HP) filter has the Sallen key architecture, the output voltage $V_1$ can be written as (*cf.* Fig. 2.15)

$$V_1 = \frac{s^2 R_{12} R_3 C_1 C_2}{s^2 R_{12} R_3 C_1 C_2 + s R_3 (C_1 + C_2) + 1} V_i \tag{2.13}$$

where $s = j\omega$, $R_{12} = 1/(1/R_1 + 1/R_2)$ and $V_i$ is the input voltage to the filter. Note that the prefix "HP_" is neglected for each parameter in order to simplify the equation.

The LP filter has the multiple feedback architecture, and the output voltage is

$$V_2 = \frac{-R_3/R_1}{s^2 R_3 R_{24} C_{12} C_3 + s[(R_{24} + R_3) C_{12} + R_{24} R_3 C_{12}/R_1] + 1} V_1 \tag{2.14}$$

where $R_{24} = 1/(1/R_2 + 1/R_4)$ and $C_{12} = C_1 + C_2$. Note that the prefix "LP_" is also neglected for each parameter in order to simplify the equation.

Based on the parameters given in [2], the bode plots of the transfer functions of the active HP, LP and the resulted BP filters are given in Fig. 2.16. The gain of the BP filter around $100k$Hz is about 13.15 dB and the passband with is about $2 * 10.416k$Hz. The stopband attenuation is about 40 dB.

The passive BP filter consists of a RC LP filter followed by a RC HP filter. Neglecting the prefix of the parameters, the voltage output of the LP filter $V_3$ can be written as

$$V_3 = \frac{1}{s R_1 C_1 + 1} V_2 \tag{2.15}$$

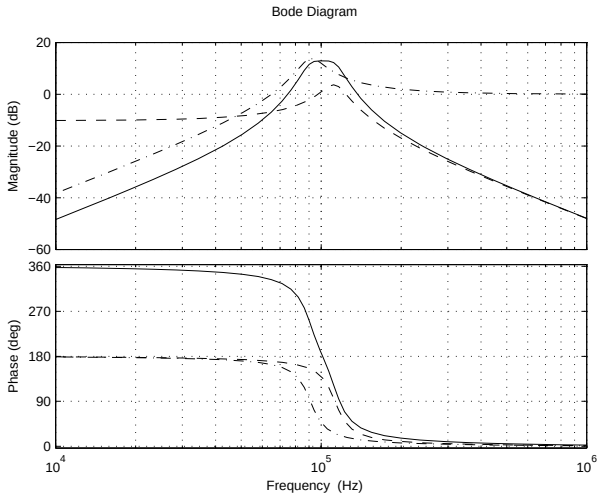


**Figure 2.16** Bode plot of the transfer functions of the active HP (dash-dot), LP (dashed) and BP (solid) filters.

and the voltage output of the HP filter $V_4$ can be written as

$$V_4 = \frac{sR_1C_1}{sR_1C_1 + 1} V_3. \tag{2.16}$$

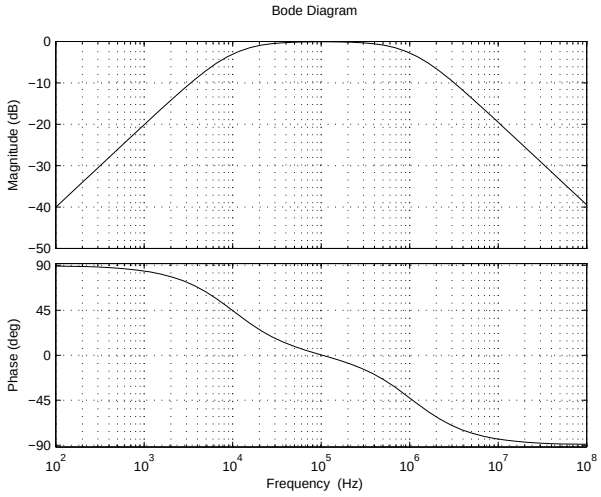


**Figure 2.17** Bode plot of the transfer function of the passive BP filters.

Based on the parameters given in [2], the bode plot of the transfer function of the resulted passive BP filter is given in Fig. 2.17. The gain of the BP filter around $100k$Hz is about 1 and the corner frequencies are around $10k$Hz and $1M$Hz.

| **Panels** | **Parameters (Unit)** | **Descriptions (Values)** |
|---|---|---|
| Input Stage (OpAmp) | $C_{Com}$ (pF) | Common mode capacitance (2) |
| | $C_{Diff}$ (pF) | Differential capacitance (1) |
| | $S_v$ (V/sqrt(Hz)) | Voltage noise density ($6 \times 10^{-9}$) |
| | $S_i$ (A/sqrt(Hz)) | Current noise density ($0.8 \times 10^{-12}$) |
| | Open Loop Gain (dB) | Open loop gain of the OpAmp (80) |
| | Input Noise Switch (1:On, 0:OFF) | Switch on or off the OpAmp noise sources |
| Middle and Output Stages (OpAmp) | $R_{Mid}$ (Ohm) | LP filter resistance ($10^5$) |
| | $C_{Mid}$ (F) | LP filter capacitance ($3.98 \times 10^{-10}$) |
| | $R_{Output}$ (Ohm) | Output resistance (55) |
| High-pass Filter | $HP\_C_1$, $HP\_C_2$ (nF) | Capacitance (1) |
| | $HP\_R_1$ (Ohm) | Resistance ($71.5 \times 10^3$) |
| | $HP\_R_2$ (Ohm) | Resistance ($22.6 \times 10^3$) |
| | $HP\_R_3$ (Ohm) | Resistance (178) |
| Low-pass Filter | $LP\_C_1$, $LP\_C_2$ (pF) | Capacitance (10) |
| | $LP\_C_3$ (nF) | Capacitance (10) |
| | $LP\_R_1$ (Ohm) | Resistance ($3.16 \times 10^3$) |
| | $LP\_R_2$ (Ohm) | Resistance ($11.5 \times 10^3$) |
| | $LP\_R_3$ (Ohm) | Resistance (976) |
| | $LP\_R_3$ (Ohm) | Resistance ($93.1 \times 10^3$) |
| | $LP\_R_4$ (Ohm) | Resistance ($11.5 \times 10^3$) |
| Passive BP Filter | $SLP\_R_1$ (Ohm) | LP resistance (150) |
| | $SLP\_C_1$ (nF) | LP capacitance (1) |
| | $SHP\_C_1$ (nF) | HP capacitance (1) |
| | $SHP\_R_1$ (Ohm) | HP resistance ($15.8 \times 10^3$) |
| | $OT\_R_1$ (Ohm) | Output buffer resistance (20) |
| | $OT\_R_2$ (Ohm) | Output buffer resistance ($15.8 \times 10^3$) |
| Others | $f_h$, $f_l$ (Hz) | Highest and lowest operation frequency ($10^6$, 1) |
| | $T$ (Kelvin) | Temperature (300) |
| | $T_s$ (s) | Sampling time ($1/(2 \times 10^6)$) |
| | Resistor Noise Switch (1:On, 0:OFF) | Switch on or off the resistor noise |

**Table 2.12** Parameters to setup in "PFM BP Filter".

### 2.2.6. Demodulator

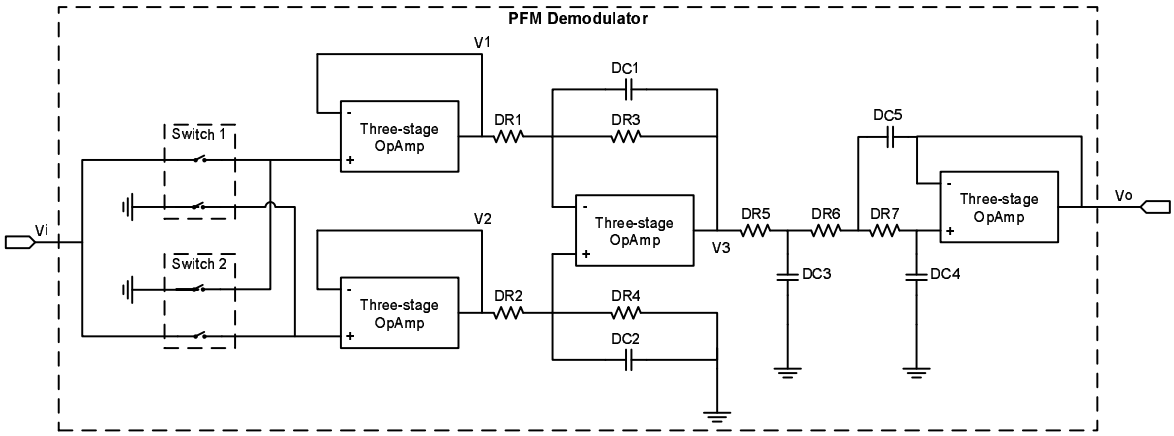


**Figure 2.18** Simscape model: "PFM Demodulator".

The "PFM Demodulator" is constructed by the "Three-stage OpAmp" in Section 2.1.3, the "Resistor with Noise" in Section 2.1.2 and the "capacitor" from the "Foundation Library\Electrical\Electrical Elements" in Simscape. The Simscape model is given in Fig. 2.18. The difference between the "PFM Demodulator (Ideal)" and "PFM Demodulator (Demodulator CMD switch)" is the control signal of the switch groups "Swtich 1" and "Switch 2". In "PFM Demodulator (Ideal)", the negative and positive sign of the the input signal are used as the control signals for the "Switch 1" and "Switch 2", respectively, in order to achieve perfect full-wave rectification. In "PFM Demodualtor (Demodulator CMD switch)", two $100k$Hz command (CMD) pulse signals with specific delays are used as the control signals for "Switch 1" and "Switch 2", which is the case in real PFM sensing hardware.

The parameters to setup in the model block dialog box are described in Table 2.13 and 2.14. The values of each parameter for the PFM hardware are also given in the table. Note that the OpAmp used in the sensing hardware is "OP484" [8].

#### Theory

The rectifier is constructed by the switches, voltage follower and differential amplifier. Then, the rectified signal passes a series of LP filters to obtain the amplitude. Assuming the OpAmp is ideal, the voltage output of the differential amplifier $V_3$ is (*cf.* Fig. 2.18)

$$V_3 = \left( \frac{R_4 \parallel \frac{1}{sC_2}}{R_2 + R_4 \parallel \frac{1}{sC_2}} \right) \left( \frac{R_1 + R_3 \parallel \frac{1}{sC_1}}{R_1} \right) V_2 - \frac{R_3 \parallel \frac{1}{sC_1}}{R_1} V_1 \tag{2.17}$$

where $s = j\omega$, "$\parallel$" denotes in parallel, $V_1$ and $V_2$ are the input voltages of the LP filter. Here, the resistors and capacitances are chosen as $R_1 = R_2$, $R_3 = R_4$ and $C_1 = C_2$, thus (2.17) becomes

$$V_3 = \frac{R_3}{R_1} \frac{1}{sR_3C_1 + 1} (V_2 - V_1). \tag{2.18}$$

Then, $V_3$ is further filtered by two LP filters and the voltage output of the demodulator $V_o$ can be written as

$$V_o = \left(\frac{1}{sR_5C_3 + 1}\right)\left(\frac{1}{s^2R_6R_7C_4C_5 + sC_4(R_6 + R_7) + 1}\right)V_3. \tag{2.19}$$

| **Panels** | **Parameters (Unit)** | **Descriptions (Values)** |
|---|---|---|
| Input Stage | $C_{Com}$ (pF) | Common mode capacitance (2) |
| (OpAmp) | $C_{Diff}$ (pF) | Differential capacitance (1) |
| | $S_v$ (V/sqrt(Hz)) | Voltage noise density ($3.9 \times 10^{-9}$) |
| | $S_i$ (A/sqrt(Hz)) | Current noise density ($0.4 \times 10^{-12}$) |
| | Open Loop Gain (dB) | Open loop gain of the OpAmp (60) |
| | Input Noise Switch (1:On, 0:OFF) | Switch on or off the OpAmp noise sources |
| Middle and | $R_{Mid}$ (Ohm) | LP filter resistance ($10^5$) |
| Output Stages | $C_{Mid}$ (F) | LP filter capacitance ($1.59 \times 10^{-10}$) |
| (OpAmp) | $R_{Output}$ (Ohm) | Output resistance (1) |
| Resistors | $DR_1$ to $DR_4$ (Ohm) | Resistance ($4.99 \times 10^3$) |
| (Demodulator) | $DR_5$ to $DR_7$ (Ohm) | Resistance ($3.24 \times 10^3$) |
| Capacitors | $DC_1$, $DC_2$ (nF) | Capacitance (1) |
| (Demodulator) | $DC_3$ to $DC_5$ (nF) | Capacitance (330) |
| Others | $R_{Switch}$ | Switch close resistance (35) |
| | $G_{Switch}$ | Switch open conductance ($10^{-13}$) |
| | $f_h$, $f_l$ (Hz) | Highest and lowest operation frequency ($10^6$, 1) |
| | $T$ (Kelvin) | Temperature (300) |
| | $T_s$ (s) | Sampling time ($1/(2 \times 10^6)$) |
| | Resistor Noise Switch (1:On, 0:OFF) | Switch on or off the resistor noise |

**Table 2.13** Parameters to setup in "PFM Demodulator (Ideal)".

| **Panels** | **Parameters (Unit)** | **Descriptions** |
|---|---|---|
| Others | Delay1 (s) | CMD signal 1 phase delay |
| | Delay2 (s) | CMD signal 2 phase delay |

**Table 2.14** Additional parameters to setup in "PFM Demodulator (Demodulator CMD switch)".

Chapter 3

# Simulink Models for the Hardware

In this chapter, in order to speed up the simulation so that the simulation of long time period could be possible, mathematic models for the PFM sensing hardware are developed and the general procedure of mathematic modeling is as follows: 1) Simplify different parts of the PFM hardware by only considering the electrical elements that affect the voltage performance, 2) Transfer function development: describe different parts of the simplified PFM hardware as voltage transfer functions, 3) Noise source development: describe the dominating noise sources in mathematics, e.g., noise sources of the transformer and transimpedance amplifiers (TIAs) in sensing hardware. Then, the simplified models for the PFM sensing hardware are built using the commonly used blocks in Simulink.

The Simulink models for the PFM actuation hardware are also presented and these models are mainly used for the simulation of the sigma-delta loop.

## 3.1. Simulink Models for IS FEE PFM Sensing Hardware

### 3.1.1. Transformer, TIAs and differential amplifier

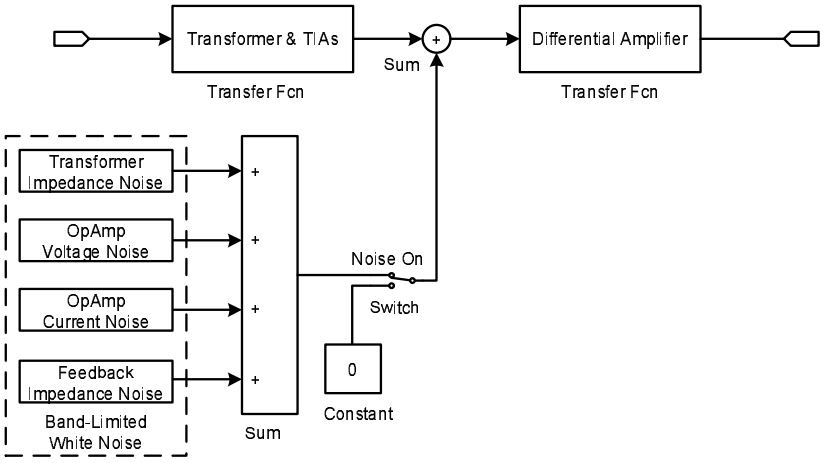


**Figure 3.1** Simunlink model: "Transformer+TIAs+Diff Amp".

The "Transformer+TIAs+Diff Amp" model is constructed by the "Transfer Fcn", "Band-Limited White Noise", "Sum", "Switch" and "Constant" blocks in Simulink, as shown in Fig. 3.1. This model is used to simulate the voltage behavior of the sensing hardware, including the transformer, TIAs and differential amplifier. The dominating noise sources from the transformer and TIAs, which are the transformer impedance noise, the OpAmp voltage and current noises, and the feedback impedance noise, are also modeled. The parameters to setup in the model block dialog box are described in Table 3.1. The values of each parameter for the PFM hardware are also given in the table. Note that the parameters of the operational amplifier (OpAmp) used in the model is from the parameters of "OP467" [5], and the parameters of the junction gate field-effect transistor (JFET) used in the model is from the parameters of "2N4393" [7]. Also note that the TIA input capacitance should be equal to the input capacitance of "2N4393".

| **Panels** | **Parameters (Unit)** | **Descriptions (Values)** |
|---|---|---|
| Transformer | $L_1$, $L_2$, $L_3$ (H) | Coil inductance ($4.2 \times 10^{-3}$) |
| | $C_1$, $C_2$ (F) | Sensing capacitance ($1.15 \times 10^{-12}$) |
| | $C_{p1}$, $C_{p2}$ (F) | Resonance tuning capacitance ($310 \times 10^{-12}$) |
| | $C_{a1}$, $C_{a2}$ (F) | Actuation capacitance ($10 \times 10^{-9}$) |
| | $Q$ | Quality factor (200) |
| | $K$ | Coupling coefficient (1) |
| TIAs | $C_{d1}$, $C_{d2}$ (F) | Decoupling capacitance ($10 \times 10^{-9}$) |
| | $A_{ov}$ (dB) | OpAmp large signal voltage gain (80) |
| | $f_c$ (Hz) | Corner frequency of $A_{ov}$ ($4 \times 10^3$) |
| | $C_i$ (F) | TIA Input capacitance ($14 \times 10^{-12}$) |
| | $D_{v1}$ (V/sqrt(Hz)) | OpAmp voltage noise density ($7 \times 10^{-9}$) |
| | $D_{v2}$ (V/sqrt(Hz)) | JFET voltage noise desnity ($3 \times 10^{-9}$) |
| | $D_i$ (A/sqrt(Hz)) | JFET gate current noise density ($2.5 \times 10^{-15}$) |
| | $R_f$ (Ohm) | Feedback resistance ($5.6 \times 10^6$) |
| | $C_f$ (F) | Feedback capacitance ($3.3 \times 10^{-12}$) |
| Differential Amplifier | $R_1$, $R_2$, $R_3$ (Ohm) | Resistance (976, 944, $18.7 \times 10^3$) |
| | $C_3$ (F) | Decoupling capacitance($10 \times 10^{-9}$) |
| | $C_4$ (F) | Capacitance ($100 \times 10^{-12}$) |
| | HR/WR Mode | HR Mode or WR Mode |
| Others | $f_h$, $f_l$ (Hz) | Highest and lowest operation frequency ($10^6$, 1) |
| | $T$ (Kelvin) | Temperature (300) |
| | $T_s$ (s) | Sampling time ($1/(8 \times 10^6)$) |
| | Noise Switch On | Switch on or off the noise sources |

**Table 3.1** Parameters to setup in "Transformer+TIAs+Diff Amp".

### Model simplification

The simplified model of the transformer with TIAs is given in Fig. 3.2. In the transfer function development, the coil resistors, the actuation circuit of the transformer and the feedback resistors of the TIAs are neglected. However, the feedback resistors of the TIAs are considered in the noise source development.

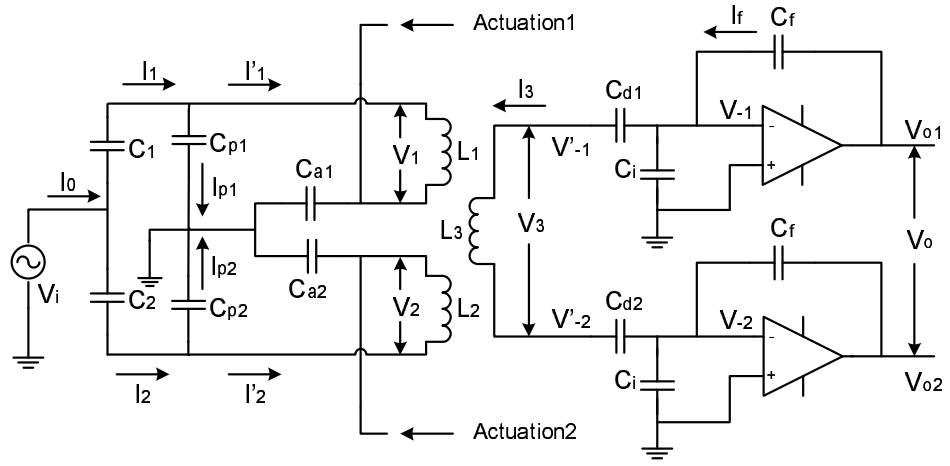


**Figure 3.2** Simplified model: "Transformer with TIAs".

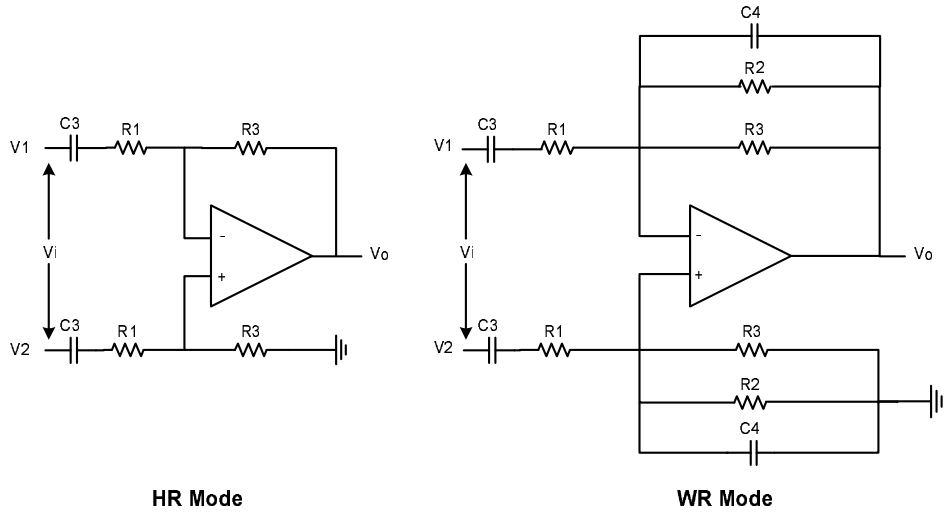


**Figure 3.3** Simplified model: "Differential Amplifier".

The simplified model of the differential amplifier is given in Fig. 3.3. In the transfer function development, the OpAmp is considered as an ideal OpAmp and the switches for the high resolution/wide range (HR/WR) mode are neglected. By defining the parameter "HR/WR Mode", the proper gain will be automatically chosen in the simulation.

### Transfer function development

The transfer function development of the transformer and TIAs is first investigated in [9]. Here, the voltage potentials at the outputs of the TIAs $V_{o1}$ and $V_{o2}$ are defined as

$$\begin{aligned} V_{o1} &= -AV_{-1} \\ V_{o2} &= -AV_{-2} \end{aligned} \tag{3.1}$$

where $A$ is the open loop gain of the OpAmp, $V_{-1}$ and $V_{-2}$ are the voltage potentials at the negative inputs of the OpAmps. Thus, the output voltage of the TIAs $V_o$ is

$$\begin{aligned} V_o &= V_{o1} - V_{o2} = -A(V_{-1} - V_{-2}) \\ &= -A[V'_{-1} + \frac{I_3}{sC_{d1}} - (V'_{-2} - \frac{I_3}{sC_{d2}})] = -A[V_3 + I_3(\frac{1}{sC_{d1}} + \frac{1}{sC_{d2}})] \end{aligned} \tag{3.2}$$

where $V_3$ is the voltage over the secondary coil of the transformer equivalent to $V'_{-1} - V'_{-2}$, as shown in Fig. 3.2. Since the voltages over the coils of the transformer are all related, we have

$$\frac{V_1}{n} = -\frac{V_2}{n} = \frac{V_3}{n_3} \tag{3.3}$$

where $V_1$ and $V_2$ are the voltages over the primary coils, $n$ and $n_3$ are the winding numbers of the primary and secondary coils, respectively. In the PFM hardware, $n$ and $n_3$ are equal to 1, thus $V_1$ and $V_2$ become (*cf.* (3.2))

$$\begin{aligned} V_1 &= \frac{n}{n_3}V_3 = -(\frac{1}{A}V_o + I_3(\frac{1}{sC_{d1}} + \frac{1}{sC_{d2}})) \\ V_2 &= -\frac{n}{n_3}V_3 = \frac{1}{A}V_o + I_3(\frac{1}{sC_{d1}} + \frac{1}{sC_{d2}}). \end{aligned} \tag{3.4}$$

The feedback current of the TIAs $I_f$ can be written as (*cf.* (3.1))

$$\begin{aligned} I_f &= sC_f(V_{o1} - V_{-1}) = sC_f\frac{1+A}{A}V_{o1} \\ I_f &= -sC_f(V_{o2} - V_{-2}) = -sC_f\frac{1+A}{A}V_{o2} \end{aligned} \tag{3.5}$$

where $C_f$ is the feedback capacitance. Adding the equations in (3.5) and dividing by 2 gives

$$I_f = \frac{1}{2}sC_f\frac{1+A}{A}(V_{o1} - V_{o2}) = \frac{1}{2}sC_f\frac{1+A}{A}V_o. \tag{3.6}$$

Consequently, the current through the secondary coil of the transformer $I_3$ can be written as

$$\begin{aligned} I_3 &= I_f - sC_iV_{-1} \\ I_3 &= I_f + sC_iV_{-2} \end{aligned} \tag{3.7}$$

where $C_i$ is the input capacitance of the OpAmp. Adding the equations in (3.7) and dividing by 2 gives (*cf.* (3.2) and (3.6))

$$I_3 = I_f - \frac{1}{2}sC_i(V_{-1} - V_{-2}) = I_f + \frac{1}{2}sC_i\frac{1}{A}V_o = \frac{1}{2}(sC_f\frac{1+A}{A} + sC_i\frac{1}{A})V_o. \tag{3.8}$$

Using the Kirchhoff's circuit laws, the currents through the primary coils of the transformer $I'_1$ and $I'_2$ can be written as

$$\begin{aligned} I'_1 &= I_1 - I_{p1} = \frac{V_i - V_1 - \frac{1}{sC_{a1}}I'_1}{\frac{1}{sC_1}} - \frac{V_1 + \frac{1}{sC_{a1}}I'_1}{\frac{1}{sC_{p1}}} \\ I'_2 &= I_2 - I_{p2} = \frac{V_i - V_2 - \frac{1}{sC_{a2}}I'_2}{\frac{1}{sC_2}} - \frac{V_2 + \frac{1}{sC_{a2}}I'_2}{\frac{1}{sC_{p2}}} \end{aligned} \tag{3.9}$$

where $V_i$ is the injection voltage of the test mass (TM), $C_1$ and $C_2$ are the sensing capacitances, $C_{p1}$ and $C_{p2}$ are the resonance tuning capacitances. Considering (3.4), $I_1'$ and $I_2'$ become

$$\begin{aligned} I_1' &= r_1 \left( sC_1V_i + (sC_1 + sC_{p1})[\frac{1}{A}V_o + I_3(\frac{1}{sC_{d1}} + \frac{1}{sC_{d2}})] \right) \\ I_2' &= r_2 \left( sC_2V_i - (sC_2 + sC_{p2})[\frac{1}{A}V_o + I_3(\frac{1}{sC_{d1}} + \frac{1}{sC_{d2}})] \right) \end{aligned} \tag{3.10}$$

where

$$r_1 = \frac{C_{a1}}{C_{a1} + C_1 + C_{p1}}, \quad r_2 = \frac{C_{a2}}{C_{a2} + C_2 + C_{p2}}. \tag{3.11}$$

Considering the mutual inductance behavior, $V_3$ can also be written as

$$V_3 = sL_3I_3 + sM_{13}I_1' - sM_{23}I_2'. \tag{3.12}$$

Here, $M_{13}$ and $M_{23}$ are the mutual inductances defined as

$$\begin{aligned} M_{13} &= K\sqrt{L_1L_3} \\ M_{23} &= K\sqrt{L_2L_3} \end{aligned} \tag{3.13}$$

where $K$ is the coupling coefficient, $L_1$, $L_2$ and $L_3$ are the inductances of the primary and secondary coils of the transformer, respectively. Substituting $I_1'$, $I_2'$, $I_3$ and $V_3$ in (3.12) by (3.10), (3.8) and (3.2), respectively, gives

$$V_o = \frac{-s^2A(M_{13}r_1C_1 - M_{23}r_2C_2)}{s^2[L_3\alpha + M_{13}r_1(C_1 + C_{p1})\beta + M_{23}r_2(C_2 + C_{p2})\beta] + \beta}V_i \tag{3.14}$$

where

$$\alpha = \frac{1}{2}[(1 + A)C_f + C_i], \quad \beta = 1 + \alpha(\frac{1}{C_{d1}} + \frac{1}{C_{d2}}). \tag{3.15}$$

Therefore, $V_o$ can be considered as the output of a filter with transfer function $\tilde{H}_1(s)$ and input signal $V_i$, where

$$\tilde{H}_1(s) = \frac{-s^2A(M_{13}r_1C_1 - M_{23}r_2C_2)}{s^2[L_3\alpha + M_{13}r_1(C_1 + C_{p1})\beta + M_{23}r_2(C_2 + C_{p2})\beta] + \beta} \tag{3.16}$$

where $\alpha$ and $\beta$ are defined in (3.15). In order to obtain more precise model, we can define the open loop gain of the OpAmp as

$$A = \frac{A_{vo}}{s\tau + 1} = \frac{A_{vo}}{s/(2\pi f_c) + 1} \tag{3.17}$$

where $A_{vo}$ is the large signal voltage gain of the OpAmp, $\tau$ is the time constant equal to $1/2\pi f_c$ and $f_c$ is the corner frequency of $A_{vo}$. Substituting $A$ in (3.16) by (3.17) gives

$$H_1(s) = \frac{b_2s^2}{a_3s^3 + a_2s^2 + a_1s + a_0} \tag{3.18}$$

where the parameters of the numerator and denominator are defined as

$$\begin{aligned} b_2 &= -A_{vo}(M_{13}r_1C_1 - M_{23}r_2C_2) \\ a_3 &= \tau[L_3\gamma + M_{13}r_1(C_1 + C_{p1})\zeta + M_{23}r_2(C_2 + C_{p2})\zeta] \\ a_2 &= L_3\alpha + M_{13}r_1(C_1 + C_{p1})\beta + M_{23}r_2(C_2 + C_{p2})\beta \\ a_1 &= \tau\zeta \\ a_0 &= \beta. \end{aligned} \tag{3.19}$$

Here, $\alpha$, $\beta$ are defined in (3.15) with $A = A_{vo}$ and

$$\gamma = \frac{1}{2}(C_f + C_i), \quad \zeta = 1 + \gamma(\frac{1}{C_{d1}} + \frac{1}{C_{d2}}). \tag{3.20}$$

Based on the parameters given in [2], the bode plot of the transfer function $H_1(s)$ is given in Fig. 3.4. Here, the sensing capacitors $C_1$ and $C_2$ are defined as $0.15p + 0.06p$F and $0.15p - 0.06p$F, respectively. As shown in the figure, the magnitude of the transfer function at $100k$Hz is about $-22.8$dB. Therefore, when the input signal $V_i$ is a $100k$Hz sinusoid signal with peak value 0.6V, the output signal $V_o$ will be a $100k$Hz sinusoid signal with peak value about $43.5m$V.

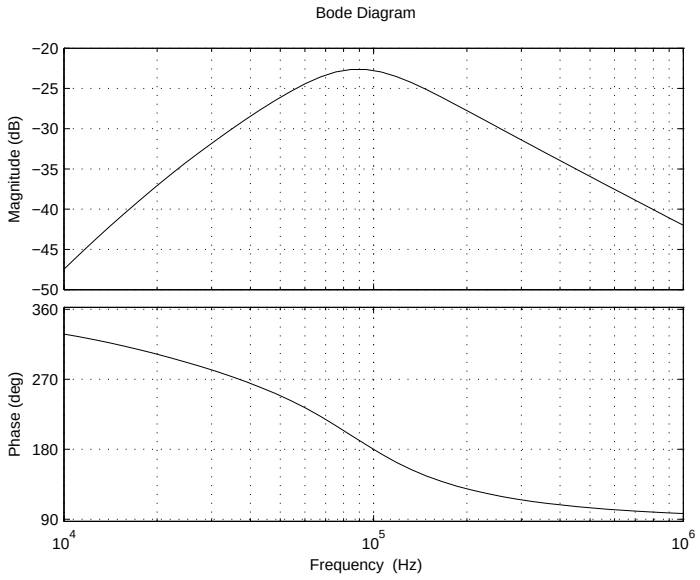


**Figure 3.4** Bode plot of the transfer function of the transformer and TIAs.

The voltage output of the differential amplifier in HR mode is (*cf.* Fig. 3.3)

$$V_o = \frac{R_3}{R_1 + \frac{1}{sC_3}}(V_2 - V_1) = \frac{sR_3C_3}{sR_1C_3 + 1}V_i = \frac{R_3}{R_1}\frac{sR_1C_3}{sR_1C_3 + 1}V_i \tag{3.21}$$

where $V_i = V_2 - V_1$. The voltage output in WR mode is

$$V_o = \frac{R_{23}||\frac{1}{sC_4}}{R_1 + \frac{1}{sC_3}}(V_2 - V_1) = \frac{sR_{23}C_3}{s^2R_1R_{23}C_3C_4 + sR_{23}C_3(R_1/R_{23} + C_4/C_3) + 1}V_i \tag{3.22}$$

where $R_{23} = 1/(1/R_2 + 1/R_3)$. Therefore, $V_o$ can be considered as the output of a filter with transfer function $H_2(s)$ and input signal $V_i$, where in HR mode

$$H_2(s) = \frac{sR_3C_3}{sR_1C_3 + 1} = \frac{R_3}{R_1}\frac{sR_1C_3}{sR_1C_3 + 1} \tag{3.23}$$

and in WR mode

$$H_2(s) = \frac{sR_{23}C_3}{s^2R_1R_{23}C_3C_4 + sR_{23}C_3(R_1/R_{23} + C_4/C_3) + 1}. \tag{3.24}$$

Based on the parameters given in [2], the bode plots of the transfer functions $H_2(s)$ in HR and WR mode are given in Fig. 3.5. As shown in the figure, the magnitude of the transfer function in HR mode at $100k$Hz is about 25.5dB, and the magnitude of the transfer function in WR mode at $100k$Hz is about $-0.84$dB. Therefore, when the input signal $V_i$ is a $100k$Hz sinusoid signal with peak value $43.47m$V - the differential output of the TIAs, the output signal $V_o$ will be a $100k$Hz sinusoid signal with peak value about $819.4m$V in HR mode.

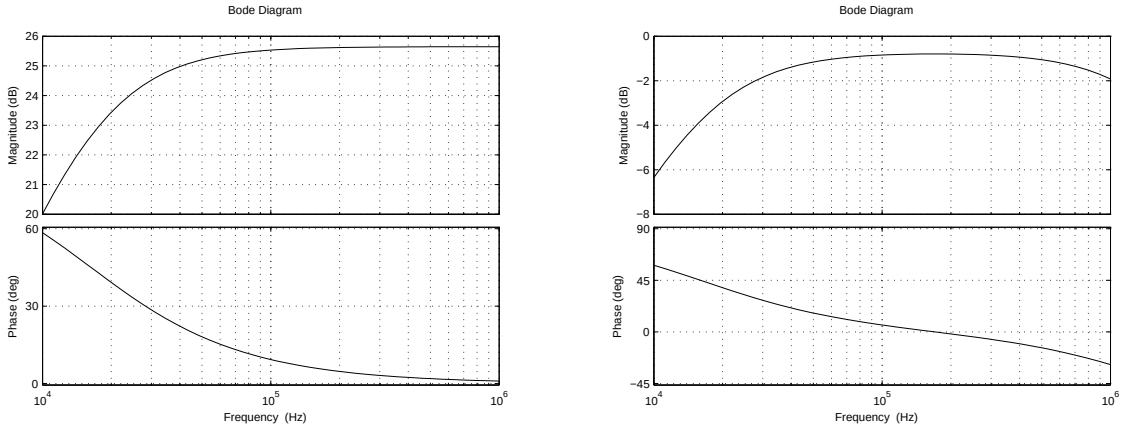


**Figure 3.5** Bode plot of the transfer function of the differential amplifier in HR mode (Left) WR mode (Right).

### Noise source development

Using the Thevenin theorem, the transformer can be equivalent to a voltage source $V_{oc}$ in series with an impedance $Z_{eq}$. The voltage source $V_{oc}$ will appear on the transformer secondary coil when the secondary coil is an open circuit - no voltage drop on $Z_{eq}$. Hence, under the open circuit condition, we have $I_3 = 0$ and (3.12) becomes

$$V_{oc} = V_3 = sM_{13}I_1' - sM_{23}I_2'. \tag{3.25}$$

Using the Kirchhoff's circuit laws, $I_1'$ and $I_2'$ can be written as

$$\begin{aligned} I_1' &= r_1(sC_1(V_i - V_{oc}) - sC_{p1}V_{oc}) \\ I_2' &= r_2(sC_2(V_i + V_{oc}) + sC_{p2}V_{oc}). \end{aligned} \tag{3.26}$$

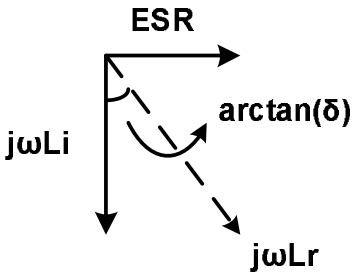


**Figure 3.6** Loss tangent of the coil $\delta$.

Substituting the currents $I_1'$ and $I_2'$ in (3.25) by (3.26) gives

$$V_{oc} = \frac{s^2(M_{13}r_1C_1 - M_{23}r_2C_2)}{s^2[M_{13}r_1(C_1 + C_{p1}) + M_{23}r_2(C_2 + C_{p2})] + 1}V_i. \tag{3.27}$$

The transformer equivalent impedance $Z_{eq}$ can be measured by shorting the secondary terminals by which the voltage source $V_{oc}$ will generate the current proportional to the impedance. Thus, assuming the output terminals are shorted, we have $V_3 = 0$ and again using the Kirchhoff's circuit laws gives

$$\begin{aligned} I_1' &= sC_1r_1V_i \\ I_2' &= sC_2r_2V_i. \end{aligned} \tag{3.28}$$

Let $V_3$ in (3.12) equal to 0, we have

$$I_3 = -\frac{s(M_{13}r_1C_1 - M_{23}r_2C_2)}{L_3}V_i. \tag{3.29}$$

Dividing $V_{oc}$ by $I_3$ gives the equivalent transformer impedance $Z_{eq}$ as (*cf.* (3.27) and (3.29))

$$Z_{eq} = |\frac{V_{oc}}{I_3}| = \frac{sL_3}{s^2[M_{13}r_1(C_1 + C_{p1}) + M_{23}r_2(C_2 + C_{p2})] + 1}. \tag{3.30}$$

In the real transformer model, there are series resistors in the coils, namely the equivalent series resistors (ESRs). The realistic inductance of the coil $L_r$ and the ideal inductance of the coil $L_i$ have the following relation

$$sL_r = ESR + sL_i \tag{3.31}$$

and the loss tangent of the coil $\delta$, shown in Fig. 3.6, is defined as

$$\delta = \frac{ESR}{|sL_i|} = \frac{ESR}{\omega L_i}. \tag{3.32}$$

Using (3.32), (3.31) can be rewritten as

$$sL_r = \delta|sL_i| + sL_i = \delta\omega L_i + sL_i \tag{3.33}$$

and thus $L_r$ becomes

$$L_r = (1 - j\delta)L_i. \tag{3.34}$$

Since the loss tangent is the ratio of the resistive power loss in the ESR to the reactive power oscillating in the coil, $\delta$ can be defined as the reciprocal of the quality factor $Q$. Hence, assuming $\delta = 1/Q$, $s = j\omega$ and substituting $L_k$ in (3.30) by $(1 - j\delta)L_k, k = 1, 2, 3$ gives

$$Z'_{eq} = \frac{j\omega(1 - j\delta)L_3}{-\omega^2(1 - j\delta)[M_{13}r_1(C_1 + C_{p1}) + M_{23}r_2(C_2 + C_{p2})] + 1}. \tag{3.35}$$

The real, imaginary and absolute values of $Z_{eq}$ versus frequency are shown in Fig. 3.7. Note that $C_{p1}$ and $C_{p2}$ are chosen as $310p$F in order to make $Z_{eq}$ achieve the maximum value at $100k$Hz. The calculation of the resonance capacitance $C_{p1}$ and $C_{p2}$ can be found in Appendix A.1.

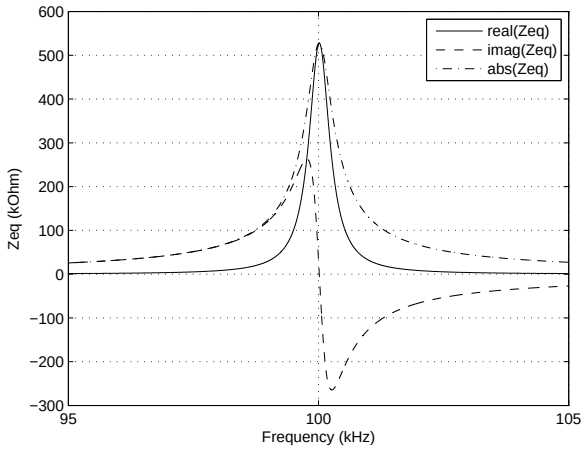


**Figure 3.7** Transformer equivalent impedance $Z_{eq}$.

Therefore, the transformer impedance noise can be considered as the thermal noise generated by the real part of $Z_{eq}$. Its power spectral density (PSD) with unit $V^2/Hz$ is defined as

$$S_{Z'_{eq}} = 4K_bT\mathsf{R}[Z'_{eq}] \tag{3.36}$$

where $K_b$ is the Boltzmann's constant equal to $1.38 \times 10^{-23}J/K$, $T$ is the temperature in Kelvin and $\mathsf{R}[.]$ denotes the real part operation.

The PSD of the transformer impedance noise at the TIAs output is then

$$S'_{Z'_{eq}} = S_{Z'_{eq}}|\frac{2Z_f}{Z_{eq'}}|^2. \tag{3.37}$$

Here, $Z_f$ is the the feedback impedance of the TIAs defined as

$$Z_f = \frac{R_f}{sR_fC_f + 1} \tag{3.38}$$

where the feedback resistor $R_f$ is considered.

The PSDs of the OpAmp and JFET voltage noise sources at the TIAs output are defined as

$$S'_v = S'_{v+} + S'_{v-} \tag{3.39}$$

where $S'_{v+}$ and $S'_{v-}$ denote the PSDs of the voltage noise sources from the OpAmp positive and negative inputs, respectively. They are defined as

$$\begin{aligned} S'_{v+} &= 2(\frac{S_{v1}}{2} + S_{v2})|1 + \frac{2Z_f}{Z'_{eq}} + \frac{Z_f}{1/sC_i}|^2 = 2(\frac{D^2_{v1}}{2} + D^2_{v2})|1 + \frac{2Z_f}{Z'_{eq}} + \frac{Z_f}{1/sC_i}|^2 \\ S'_{v-} &= 2(\frac{S_{v1}}{2} + S_{v2})|1 + \frac{2Z_f}{Z'_{eq}}|^2 = 2(\frac{D^2_{v1}}{2} + D^2_{v2})|1 + \frac{2Z_f}{Z'_{eq}}|^2. \end{aligned} \tag{3.40}$$

where $S_{v1}$ and $S_{v2}$ are the PSDs of the OpAmp and JFET voltage noise sources with unit $V^2/Hz$, respectively. The PSD of the OpAmp noise source is equivalent to $D^2_{v1}$, where $D_{v1}$ is the OpAmp voltage noise density given in the datasheet with unit $V/\sqrt{Hz}$. Normally, the OpAmp voltage noise source is only considered at the positive input for the sake of simplicity and the PSD $S_{v1}$ is double of the real value. In order to obtain more accurate model, we consider the voltage noise sources at both positive and negative inputs. Hence, the PSD of the OpAmp voltage noise sources should be half of the value based on the datasheet, i.e., $S_{v1}/2 = D^2_{v1}/2$.

Since the OpAmp current sources are isolated from the TIA feedback by the JFETs, the only current noise source we considered in the model is the JFET gate current noise source. The PSD of the JFET current noise source at the TIAs output is defined as

$$S'_i = 2S_i|Z_f|^2 = 2D^2_i|Z_f|^2 \tag{3.41}$$

where $S_i$ is the PSD of the JFET gate current noise source with unit $A^2/Hz$. The value of $S_i$ is equivalent to $D^2_i$, where $D_i$ is the JFET gate current noise density with unit $A/\sqrt{Hz}$. $D_i$ is usually very small, e.g., in the range of $10^{-15}A/\sqrt{Hz}$.

The PSD of the thermal noise of the feedback impedance $Z_f$ at the TIAs output is defined as

$$S'_{Z_f} = 2 \times 4K_bT\mathsf{R}[Z_f]. \tag{3.42}$$

The development of the PSDs of the noise sources at the TIAs output are given in Appendix A.2. The amplitude spectral densities (ASDs) of these noise sources are shown in Fig. 3.8, and the ASDs of the noise sources are defined as in Table. 3.2.

| Noise Sources | ASDs | Reference |
|---|---|---|
| Transformer impedance noise | $\sqrt{S'_{Z'_{eq}}}$ | (3.37) |
| Voltage noise at Amp + | $\sqrt{S'_{v+}}$ | (3.40) |
| Voltage noise at OpAmp - | $\sqrt{S'_{v-}}$ | (3.40) |
| JFET gate current noise | $\sqrt{S'_i}$ | (3.41) |
| Feedback impedance noise | $\sqrt{S'_{Z_f}}$ | (3.42) |

**Table 3.2** Definition of the ASDs of the noise sources.

Since the dominating noise is from the transformer and TIAs, other noise sources such as the resistor thermal noise in the differential amplifier etc. are neglected.

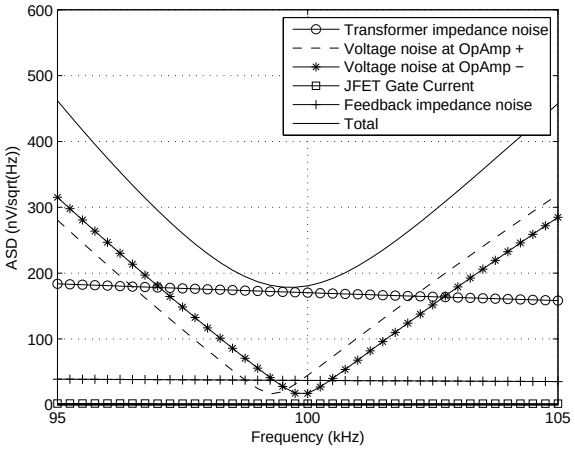


**Figure 3.8** ASDs of the noise sources at the TIAs output.

### Simulink modeling

The transformer followed by two TIAs is modeled using the "Transfer Fcn" block in Simulink, where the numerator and denominator of the transfer function are defined in (3.18). The differential amplifier is also modeled using the "Transfer Fcn" block, where the numerator and denominator are defined in (3.23) and (3.24).

All the noise sources are modeled using the "Band-Limited White Noise" block in Simulink, and the powers of the noise sources are defined as in Table. 3.3, where $T_s$ is the sampling time, $f_h$ and $f_l$ are the highest and lowest operation frequency, respectively.

| Noise Sources | Power | Reference |
|---|---|---|
| Transformer impedance noise | $T_s \int_{f_l}^{f_h} S'_{Z'_{eq}} df$ | (3.37) |
| Voltage noise source | $T_s \int_{f_l}^{f_h} S'_v df$ | (3.39) |
| Current noise source | $T_s \int_{f_l}^{f_h} S'_i df$ | (3.41) |
| Feedback impedance noise | $T_s \int_{f_l}^{f_h} S'_{Z_f} df$ | (3.42) |

**Table 3.3** Definition of the noise source power in "Transformer+TIAs+Diff Amp".

### 3.1.2. Bandpass filter

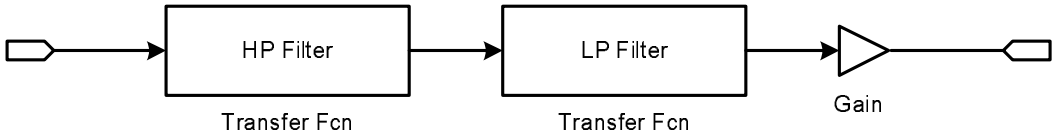


**Figure 3.9** Simunlink model: "Band Pass Filter".

The "Band Pass Filter" (BP Filter) model is constructed by the "Transfer Fcn" and "Gain" blocks in Simulink, as shown in Fig. 3.9. This model is used to simulate the voltage behavior of the BP Filter, consisting of a high pass (HP) filter followed by a low pass (LP) filter and a gain compensation. The gain compensation is used to compensate the output voltage level, in order to achieve the same voltage output value as the real PFM hardware. There is no noise source in the model, since the noise is negligible compared to the noise from the transformer and TIAs. The parameters to setup in the model block dialog box are described in Table 3.4. The values of each parameter for the PFM hardware are also given in the table.

| **Panels** | **Parameters (Unit)** | **Descriptions (Values)** |
|---|---|---|
| High Pass Filter | $R_1$, $R_2$, $R_3$ (Ohm) | Resistance ($22.6 \times 10^3$, $71.5 \times 10^3$, 178) |
| | $C_1$, $C_2$ (F) | Capacitance ($10^{-9}$) |
| Low Pass Filter | $R_1$ to $R_5$ (Ohm) | Resistance ($3.16 \times 10^3$, $11.5 \times 10^3$, 976, $93.1 \times 10^3$, $11.5 \times 10^3$) |
| | $C_1$, $C_2$, $C_3$ (F) | Capacitance ($10 \times 10^{-12}$, $10 \times 10^{-12}$, $10 \times 10^{-9}$) |
| | Gain Compensation | Compensate the gain of the BP Filter (1.1783) |

**Table 3.4** Parameters to setup in "Band Pass Filter".

#### Model simplification

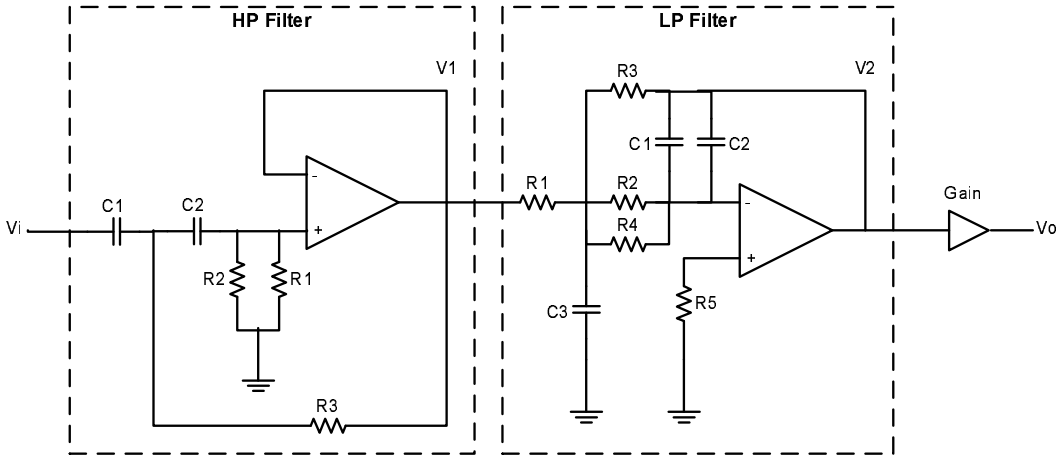


**Figure 3.10** Simplified model: "Band Pass Filter".

The simplified model of the BP filter is given in Fig. 3.10. In the transfer function development, the OpAmps are considered to be ideal. The passive BP filter and the output stage are replaced by a voltage gain block, since they only contributed to the gain of the voltage in the real hardware.

### Transfer function development

The voltage output of the HP filter $V_1$ can be written as (*cf.* Fig. 3.10)

$$V_1 = \frac{s^2 R_{12} R_3 C_1 C_2}{s^2 R_{12} R_3 C_1 C_2 + s R_3 (C_1 + C_2) + 1} V_i \tag{3.43}$$

where $R_{12} = 1/(1/R1 + 1/R2)$ and $V_i$ is the voltage input to the filter. Therefore, $V_1$ can be considered as the output of a filter with transfer function $H_3(s)$ defined as

$$H_3(s) = \frac{s^2 R_{12} R_3 C_1 C_2}{s^2 R_{12} R_3 C_1 C_2 + s R_3 (C_1 + C_2) + 1} \tag{3.44}$$

The voltage output of the LP filter $V_2$ is

$$V_2 = \frac{-R_3/R_1}{s^2 R_3 R_{24} C_{12} C_3 + s[(R_{24} + R_3) C_{12} + R_{24} R_3 C_{12}/R_1] + 1} V_1 \tag{3.45}$$

where $R_{24} = 1/(1/R_2 + 1/R_4)$ and $C_{12} = C_1 + C_2$. Therefore, $V_2$ can be considered as the output of a filter with transfer function $H_4(s)$ defined as

$$H_4(s) = \frac{-R_3/R_1}{s^2 R_3 R_{24} C_{12} C_3 + s[(R_{24} + R_3) C_{12} + R_{24} R_3 C_{12}/R_1] + 1} \tag{3.46}$$

Based on the parameters given in [2], the bode plots of the transfer functions of the active HP, LP and the resulted BP filters are given in Fig. 3.11. The gain of the BP filter around $100k$Hz is about 13.15 dB and the passband with is about $2 * 10.416k$Hz. The stopband attenuation is about 40 dB.

### Noise source development

Noise sources in the BP filter are ignored, since the noise is negligible compared to the noise from the transformer and TIAs.

### Simulink modeling

The HP filter is modeled using the "Transfer Fcn" block in Simulink, where the numerator and denominator of the transfer function are defined in (3.44). The LP filter is also modeled using the "Transfer Fcn" block, where the numerator and denominator are defined in (3.46). The value of the "Gain" is defined by comparing the BP filter voltage output with the real hardware output.

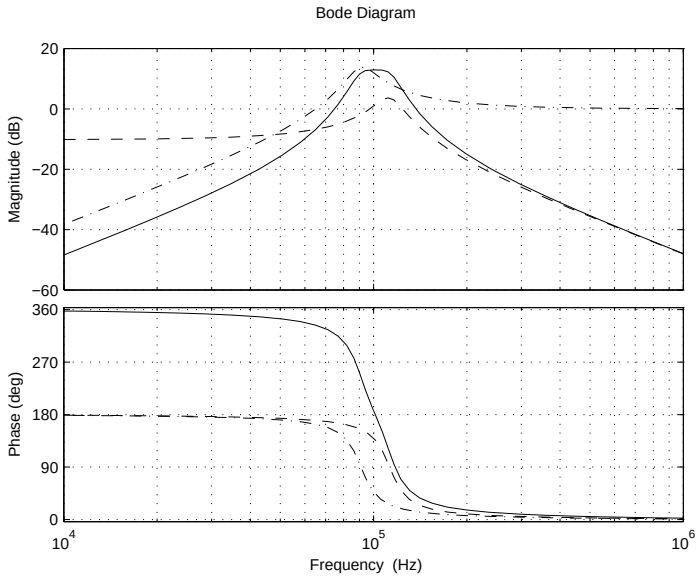


**Figure 3.11** Bode plot of the transfer functions $H_3(s)$ (dash-dot), $H_4(s)$ (dashed) and $H_3(s)H_4(s)$.

### 3.1.3. Demodulator

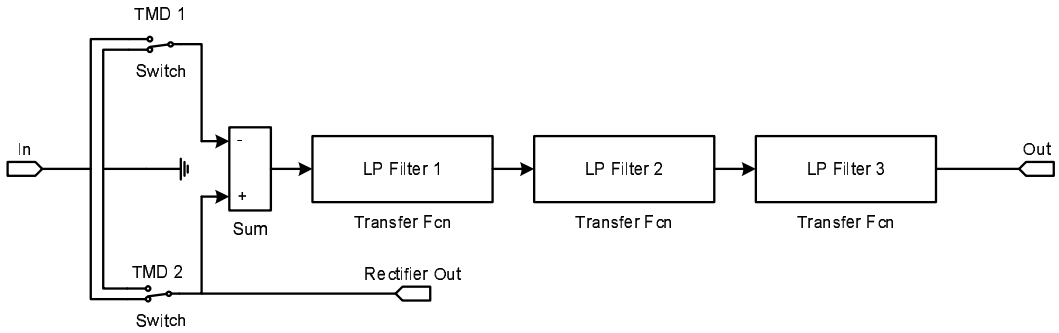


**Figure 3.12** Simunlink model: "Demodulator".

The "Demodulator" model is constructed by the "Transfer Fcn", "Switch", "Ground" and "Sum" blocks in Simulink, as shown in Fig. 3.12. This model is used to simulate the voltage behavior of the demodulator with command (CMD) pulse signals. The parameters to setup in the model block dialog box are described in Table 3.5. The values of each parameter for the PFM hardware are also given in the table.

| Panels | Parameters (Unit) | Descriptions (Values) |
|---|---|---|
| Low Pass | $R_1$ (Ohm) | Resistance (499) |
| Filter 1 | $C_1$ (F) | Capacitance ($10^{-9}$) |
| Low Pass | $R_2$ (Ohm) | Resistance ($3.24 \times 10^3$) |
| Filter 2 | $C_2$ (F) | Capacitance ($330 \times 10^{-9}$) |
| Low Pass | $R_3$, $R_4$ (Ohm) | Resistance ($3.24 \times 10^3$) |
| Filter 3 | $C_3$, $C_4$ (F) | Capacitance ($330 \times 10^{-9}$) |

**Table 3.5** Parameters to setup in "Demodulator".

#### Model simplification

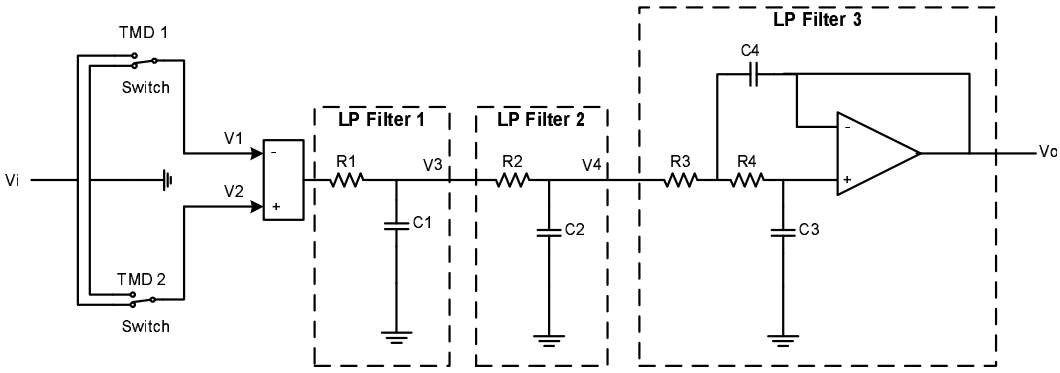


**Figure 3.13** Simplified model: "Demodulator".

The simplified model of the demodulator is given in Fig. 3.13. In the transfer function development, the OpAmps are considered to be ideal. The voltage followers are neglected, and the followed LP filter is simplified to a RC LP filter - "LP Filter 1".

### Transfer function development

The voltage output of the "LP Filter 1" $V_3$ is (*cf.* Fig. 3.13)

$$V_3 = \frac{1}{sR_1C_1 + 1}(V_2 - V_1) = \frac{1}{sR_1C_1 + 1}|V_i| = H_5(s)|V_i| \tag{3.47}$$

where the rectifier output $|V_i| = V_2 - V_1$ and $H_5(s) = 1/(sR_1C_1 + 1)$. Therefore, $V_3$ can be considered as the output of the filter with transfer function $H_5(s)$. $V_3$ is further filtered by other two LP filters and similarly, the output signal $V_o$ can also be considered as the output of the filter with transfer function $H_6(s)$, defined as

$$V_o = H_6(s)V_3 = \left(\frac{1}{sR_2C_2 + 1}\right)\left(\frac{1}{s^2R_3R_4C_3C_4 + sC_4(R_3 + R_4) + 1}\right)V_3. \tag{3.48}$$

Based on the parameters given in [2], the bode plot of the transfer functions $H_5(s)H_6(s)$ is given in Fig. 3.14.

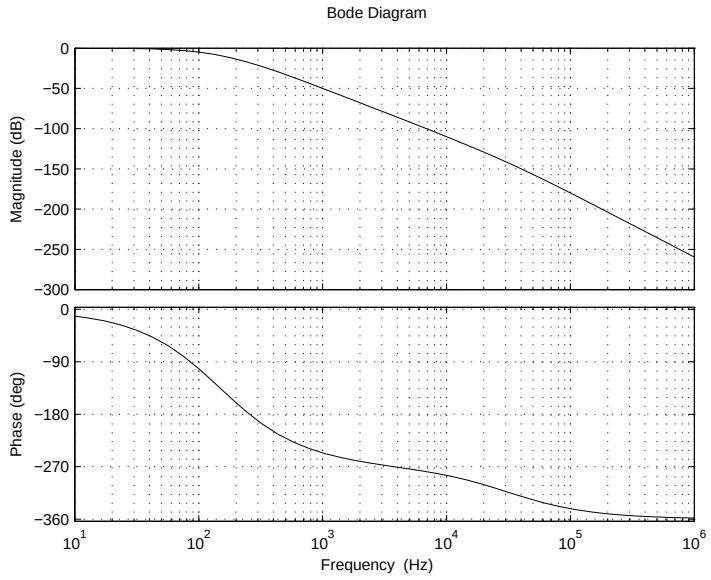


**Figure 3.14** Bode plot of the transfer functions $H_5(s)H_6(s)$.

### Noise source development

Noise sources in the demodulator are ignored, since the noise here is not the dominating noise in the hardware.

### Simulink modeling

The LP filters are modeled using the "Transfer Fcn" blocks in Simulink, where the numerators and denominators of the transfer functions are defined in (3.47) and (3.48).

### 3.1.4. ADC

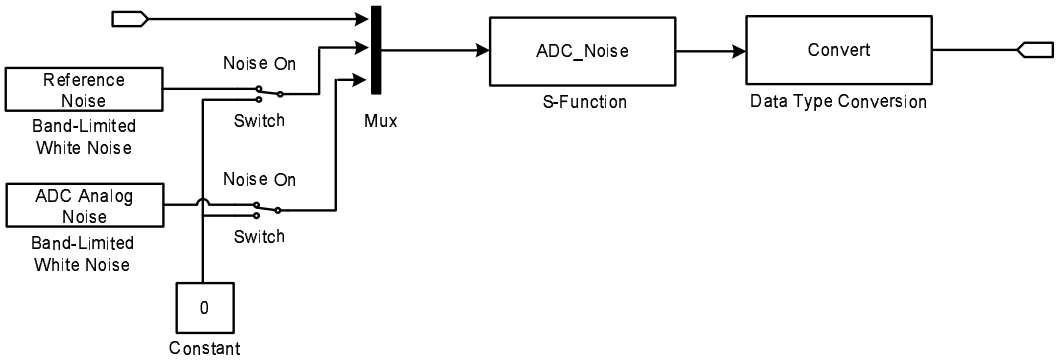


**Figure 3.15** Simunlink model: "ADC (+Noise)".

The "ADC (+Noise)" model is constructed by the "S-Function", "Band-Limited White Noise", "Uniform Random Number", "Data Type Converting","Mux", "Sum", "Switch" and "Constant" blocks in Simulink, as shown in Fig. 3.15. This model is used to simulate the ADC with non-perfect voltage reference modeled as the voltage reference noise and limited resolution modeled as the resolution noise and quantization noise. The parameters to setup in the model block dialog box are described in Table 3.6. The values of each parameter for the PFM hardware are also given in the table.

| **Parameters (Unit)** | **Descriptions (Values)** |
|---|---|
| $N$ (Bits) | Number of converting bits (16) |
| $V_{ref}$ (V) | Reference Voltage (2.5) |
| $SINAD$ (dB) | Signal to noise and distortion ratio (86) |
| $Var_{ref}$ ($V^2$) | Variance of the voltage reference noise ($(10^{-3})^2$) |
| $T_s$ (s) | Sampling time ($1/(8 \times 10^6)$) |
| Neg_Out | Switch on or off negative output values of ADC |
| Noise Switch On | Switch on or off the reference and quantization noises |

**Table 3.6** Parameters to setup in "ADC (+Noise)".

#### Model description

The "S-Function" block is used to model the behavior of the analog-to-digital Converter (ADC) with different noises. The "S-Function" has three input arguments, which are the voltage input $V_i$, the voltage reference noise $N_{ref}$ and the resolution noise $N_{res}$. The parameters of the "S-Function" includes the number of converting bits $N$ and reference voltage $V_{ref}$, etc. The output of the "S-Function" $V_o$ with quantization noise provides the output of the model.

The flowchart of the "S-Function" is shown in Fig. 3.16. The maximum and minimum voltages of the ADC are

$$\begin{aligned} V_{max} &= V_{ref} + N_{ref} \\ V_{min} &= -(V_{ref} + N_{ref}) \end{aligned} \tag{3.49}$$

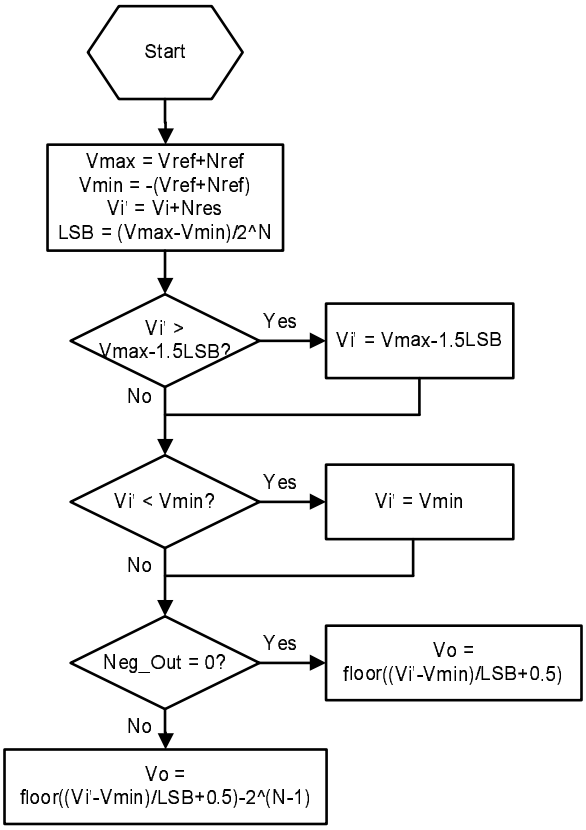


**Figure 3.16** Flowchart of the "S-Function" for "ADC with Noise".

where $N_{ref}$ is modeled as an additive white Gaussian noise (AWGN) and the variance of $N_{ref}$ is defined by the variance of the voltage reference noise $Var_{ref}$. In our simulation, $Var_{ref}$ is defined as

$$Var_{ref} = \left(PSD \times \sqrt{BW}\right)^2 \tag{3.50}$$

where $PSD$ is the power spectral density of the voltage reference noise with unit $V/\sqrt{Hz}$ and $BW$ denotes the bandwidth with unit $Hz$.

The input signal for conversion is

$$V_i' = V_i + N_{res} \tag{3.51}$$

where $V_i$ is the input signal of the ADC and $N_{res}$ is the ADC analog noise. The variance of the ADC analog noise $Var_{res}$ is defined as

$$Var_{res} = ((N - ENOB) * LSB)^2 \tag{3.52}$$

where $LSB$ denotes the least significant bit defined as

$$LSB = \frac{2 \times V_{ref}}{2^N} \tag{3.53}$$

and $ENOB$ denotes the effective number of bits, calculated as

$$ENOB = \frac{SINAD - 1.76}{6.02}. \tag{3.54}$$

Here, $SINAD$ denotes signal to noise and distortion ratio. The detail of the $ENOB$ and $SINAD$ can be found in [10].

### 3.1.5. Transformer, TIAs and differential amplifier for actuation

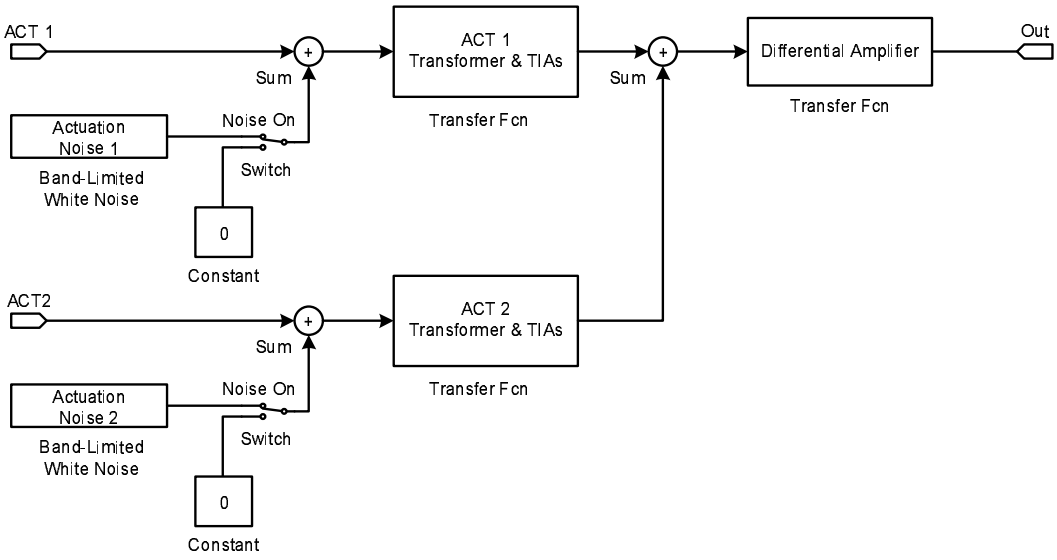


**Figure 3.17** Simunlink model: "Transformer+TIAs+Diff Amp for Actuation".

The "Transformer+TIAs+Diff Amp for Actuation" model is constructed by the "Transfer Fcn", "Band-Limited White Noise", "Sum", "Switch" and "Constant" blocks in Simulink, as shown in Fig. 3.17. This model is used to simulate the voltage reaction of the sensing hardware to the actuation signal and noise. The parameters to setup in the model block dialog box are described in Table 3.7. The values of each parameter for the PFM hardware are also given in the table. Note that the parameters of the OpAmp used in the model is from "OP467" [5], and the parameters of the JFET used in the model is from the parameters of "2N4393" [7]. Also note that the TIA input capacitance should be equal to the input capacitance of "2N4393".

#### Model simplification

The simplified model of the transformer with TIAs for actuation is given in Fig. 3.18. In the transfer function development, the actuation circuit of the transformer is neglected and the actuation inputs are considered as two AC voltage inputs. The coil resistors and the feedback resistor of the TIA are also neglected. However, the resistors of the actuation circuit are considered in the noise source development. The simplified model of the differential amplifier is similar as in Fig. 3.3.

#### Transfer function development

The voltage potentials at the output of the TIAs $V_{o1}$ and $V_{o2}$ are

$$\begin{aligned} V_{o1} &= -AV_{-1} \\ V_{o2} &= -AV_{-2} \end{aligned} \tag{3.55}$$

where $A$ is the open loop gain of the OpAmp at the operation frequency, $V_{-1}$ and $V_{-2}$ are the voltage potentials at the negative inputs of the OpAmps. Thus, the output voltage of

| Panels | Parameters (Unit) | Descriptions (Values) |
|---|---|---|
| Transformer | $L_1$, $L_2$, $L_3$ (H) | Coil inductance ($4.2 \times 10^3$) |
| | $C_1$, $C_2$ (F) | Sensing capacitance ($1.15 \times 10^{-12}$) |
| | $C_{p1}$, $C_{p2}$ (F) | Input capacitance ($310 \times 10^{-12}$) |
| | $K$ | Coupling coefficient (1) |
| | $R$ (Ohm) | Actuation resistance ($3.3 \times 10^3$) |
| | $C$ (F) | Actuation capacitance ($10 \times 10^{-9}$) |
| TIAs | $C_{d1}$, $C_{d2}$ (F) | Decoupling capacitance ($10 \times 10^{-9}$) |
| | $A_{ov}$ (dB) | OpAmp large signal voltage gain (80) |
| | $f_c$ (Hz) | Corner frequency of $A_{ov}$ ($4 \times 10^3$) |
| | $C_{in}$ | TIA Input capacitance ($14 \times 10^{-12}$) |
| | $R_f$ (Ohm) | Feedback resistance ($5.6 \times 10^6$) |
| | $C_f$ (F) | Feedback capacitance ($3.3 \times 10^{-12}$) |
| Differential Amplifier | $R_1$, $R_2$, $R_3$ (Ohm) | Resistance (976, 944, $18.7 \times 10^3$) |
| | $C_3$ (F) | Decoupling capacitance($10 \times 10^{-9}$) |
| | $C_4$ (F) | Capacitance ($100 \times 10^{-12}$) |
| | HR/WR Mode | HR Mode or WR Mode |
| Others | $f_h$, $f_l$ (Hz) | Highest and lowest operation frequency ($10^6$, 1) |
| | $T$ (Kelvin) | Temperature (300) |
| | $T_s$ (s) | Sampling time ($1/(8 \times 10^6)$) |
| | Noise Switch On | Switch on or off the noise sources |

**Table 3.7** Parameters to setup in "Transformer+TIAs+Diff Amp for Actuation".

the TIAs $V_o$ is

$$\begin{aligned} V_o &= V_{o1} - V_{o2} = -A(V_{-1} - V_{-2}) \\ &= -A[V'_{-1} + \frac{I_3}{sC_{d1}} - (V'_{-2} - \frac{I_3}{sC_{d2}})] = -A[V_{L3} + I_3(\frac{1}{sC_{d1}} + \frac{1}{sC_{d2}})] \end{aligned} \tag{3.56}$$

where $V_{L3}$ is the voltage over the secondary coil of the transformer equivalent to $V'_{-1} - V'_{-2}$, as shown in Fig. 3.18. Since the voltages over the coils of the transformer are all related

$$\frac{V_{L1}}{n} = -\frac{V_{L2}}{n} = \frac{V_{L3}}{n_3} \tag{3.57}$$

where $n$ and $n_3$ are the winding numbers of the primary and secondary coils, respectively. In the PFM hardware, $n$ and $n_3$ are equal to 1, thus the voltages over the primary coils $V_{L1}$ and $V_{L2}$ are (*cf.* (3.56))

$$\begin{aligned} V_{L1} &= \frac{n}{n_3} V_{L3} = -(\frac{1}{A} V_o + I_3(\frac{1}{sC_{d1}} + \frac{1}{sC_{d2}})) \\ V_{L2} &= -\frac{n}{n_3} V_{L3} = \frac{1}{A} V_o + I_3(\frac{1}{sC_{d1}} + \frac{1}{sC_{d2}}). \end{aligned} \tag{3.58}$$

The feedback current of the TIAs $I_f$ can be written as

$$\begin{aligned} I_f &= sC_f(V_{o1} - V_{-1}) = sC_f \frac{1+A}{A} V_{o1} \\ I_f &= -sC_f(V_{o2} - V_{-2}) = -sC_f \frac{1+A}{A} V_{o2} \end{aligned} \tag{3.59}$$

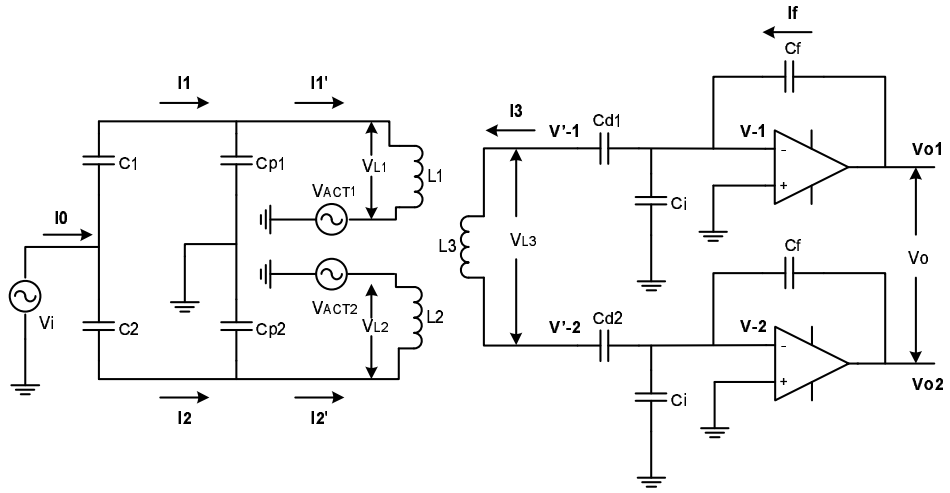


**Figure 3.18** Simplified model: "Transformer with TIAs for Actuation".

where $C_f$ is the feedback capacitance. Adding the equations in (3.59) and dividing by 2 gives

$$I_f = \frac{1}{2} sC_f \frac{1+A}{A}(V_{o1} - V_{o2}) = \frac{1}{2} sC_f \frac{1+A}{A} V_o. \tag{3.60}$$

Consequently, the current through the secondary coil of the transformer $I_3$ can be written as

$$\begin{aligned} I_3 &= I_f - sC_i V_{-1} \\ I_3 &= I_f + sC_i V_{-2} \end{aligned} \tag{3.61}$$

where $C_i$ is the input capacitance of the OpAmp. Adding the equations in (3.61) and dividing by 2 gives (*cf.* (3.56) and (3.60))

$$I_3 = I_f - \frac{1}{2} sC_i(V_{-1} - V_{-2}) = I_f + \frac{1}{2} sC_i \frac{1}{A} V_o = \frac{1}{2}(sC_f \frac{1+A}{A} + sC_i \frac{1}{A}) V_o. \tag{3.62}$$

Using the Kirchhoff's circuit laws, the currents through the primary coils of the transformer $I_1'$ and $I_2'$ can be written as (*cf.* (3.58))

$$\begin{aligned} I_1' &= sC_1(V_i - V_{L1} - V_{ACT1}) - sC_{p1}(V_{L1} + V_{ACT1}) \\ &= sC_1 V_i + (sC_1 + sC_{p1})(\frac{1}{A} V_o + I_3(\frac{1}{sC_{d1}} + \frac{1}{sC_{d2}})) - (sC_1 + sC_{p1}) V_{ACT1} \\ I_2' &= sC_2(V_i - V_{L2} - V_{ACT2}) - sC_{p2}(V_{L2} + V_{ACT2}) \\ &= sC_2 V_i - (sC_2 + sC_{p2})(\frac{1}{A} V_o + I_3(\frac{1}{sC_{d1}} + \frac{1}{sC_{d2}})) - (sC_2 + sC_{p2}) V_{ACT2} \end{aligned} \tag{3.63}$$

where $V_i$ is the attenuated injection voltage, $V_{ACT1}$ and $V_{ACT2}$ are the actuation voltage inputs, $C_1$ and $C_2$ are the sensing capacitances, $C_{p1}$ and $C_{p2}$ are the resonance tuning capacitances of the transformer.

Considering the mutual inductance behavior, $V_3$ can also be written as

$$V_{L3} = sL_3 I_3 + sK\sqrt{L_1 L_3} I_1' - sK\sqrt{L_2 L_3} I_2' \tag{3.64}$$

where $K$ is the coupling coefficient, $L_1$, $L_2$ and $L_3$ are the inductances of the primary and secondary coils of the transformer, respectively. Assuming $V_i = 0$ and substituting the $I_1'$ and $I_2'$ in (3.64) by (3.61) and (3.63) gives

$$V_o = \frac{s^2 A[K\sqrt{L_1L_3}(C_1 + C_{p1})V_{ACT1} - K\sqrt{L_2L_3}(C_2 + C_{p2})V_{ACT2}]}{s^2[L_3\alpha + K\sqrt{L_1L_3}(C_1 + C_{p1})\beta + K\sqrt{L_2L_3}(C_2 + C_{p2})\beta] + \beta} \tag{3.65}$$

where

$$\alpha = \frac{1}{2}[(1 + A)C_f + C_i], \quad \beta = 1 + \alpha(\frac{1}{C_{d1}} + \frac{1}{C_{d2}}). \tag{3.66}$$

Therefore, $V_o$ can be considered as the difference between the output of the filter $\tilde{H}_1$ with input $V_{ACT1}$ and the output of the filter $\tilde{H}_2$ with input $V_{ACT2}$, where the transfer functions of the filters are

$$\begin{aligned} \tilde{H}_1(s) &= \frac{s^2 AK\sqrt{L_1L_3}(C_1 + C_{p1})}{s^2[L_3\alpha + K\sqrt{L_1L_3}(C_1 + C_{p1})\beta + K\sqrt{L_2L_3}(C_2 + C_{p2})\beta] + \beta} \\ \tilde{H}_2(s) &= \frac{s^2 AK\sqrt{L_2L_3}(C_2 + C_{p2})}{s^2[L_3\alpha + K\sqrt{L_1L_3}(C_1 + C_{p1})\beta + K\sqrt{L_2L_3}(C_2 + C_{p2})\beta] + \beta} \end{aligned} \tag{3.67}$$

where $\alpha$ and $\beta$ are defined in (3.66). Furthermore, we can define the open loop gain of the OpAmp as

$$A = \frac{A_{vo}}{s\tau + 1} = \frac{A_{vo}}{s/(2\pi f_c) + 1} \tag{3.68}$$

where $A_{vo}$ is the large signal voltage gain of the OpAmp, $\tau$ is the time constant equal to $1/2\pi f_c$ and $f_c$ is the corner frequency of $A_{vo}$. Substituting $A$ in (3.67) by (3.68) gives

$$\begin{aligned} H_1(s) &= \frac{b_{21}s^2}{a_3s^3 + a_2s^2 + a_1s + a_0} \\ H_2(s) &= \frac{b_{22}s^2}{a_3s^3 + a_2s^2 + a_1s + a_0} \end{aligned} \tag{3.69}$$

where the parameters of the numerator and denominator are defined as

$$\begin{aligned} b_{21} &= A_{vo}K\sqrt{L_1L_3}(C_1 + C_{p1}) \\ b_{22} &= A_{vo}K\sqrt{L_2L_3}(C_2 + C_{p2}) \\ a_3 &= \tau[L_3\gamma + K\sqrt{L_1L_3}(C_1 + C_{p1})\zeta + K\sqrt{L_2L_3}(C_2 + C_{p2})\zeta] \\ a_2 &= L_3\alpha + K\sqrt{L_1L_3}(C_1 + C_{p1})\beta + K\sqrt{L_2L_3}(C_2 + C_{p2})\beta \\ a_1 &= \tau\zeta \\ a_0 &= \beta. \end{aligned} \tag{3.70}$$

Here, $\alpha$, $\beta$ are defined in (3.66) with $A = A_{vo}$ and

$$\gamma = \frac{1}{2}(C_f + C_i), \quad \zeta = 1 + \gamma(\frac{1}{C_{d1}} + \frac{1}{C_{d2}}). \tag{3.71}$$

Based on the parameters given in [2], the bode plots of the transfer function $H_1(s)$ and $H_2(s)$ are given in Fig. 3.19. Here, the sensing capacitors $C_1$ and $C_2$ are defined as $0.15p + 0.06p$F and $0.15p - 0.06p$F, respectively. As shown in the figure, the magnitude of the transfer functions at $100k$Hz is about 45.2dB.

The transfer function development of the differential amplifier is equivalent to the development in Section 3.1.1.

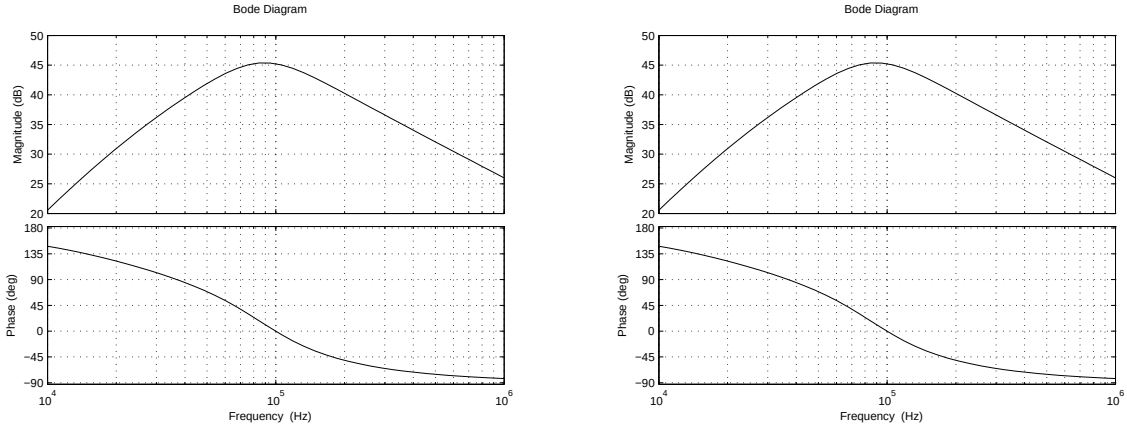


**Figure 3.19** Bode plot of the transfer function $H_1(s)$ (Left) and $H_2(s)$ (Right).

### Noise source development

Since the noise sources of the transformer and TIAs have already been developed in Section 3.1.1, we only need to consider the thermal noise of the impedances in the actuation circuit. The PSD of the thermal noise of the actuation impedance $Z_A$ is defined as

$$S_{Z_A} = 4K_bT\mathsf{R}[Z_A] \tag{3.72}$$

where

$$Z_A = \frac{R}{sRC+1}. \tag{3.73}$$

Here, $R$ and $C$ are the resistor and capacitor in the actuation circuit, respectively.

### Simulink modeling

The transformer followed by two TIAs for actuation is modeled using the "Transfer Fcn" block in Simulink, where the numerators and denominators of the transfer functions are defined in (3.69). The differential amplifier is also modeled using the "Transfer Fcn" block, where the numerator and denominator are defined in (3.23) and (3.24).

The noise source is modeled using the "Band-Limited White Noise" block in Simulink, and the powers of the noise sources are defined as $\int_{f_l}^{f_h} S_{Z_A} df \times T_s$, where $T_s$ is the sampling time and $S_{Z_A}$ is defined in (3.72).

### 3.1.6. Input generator

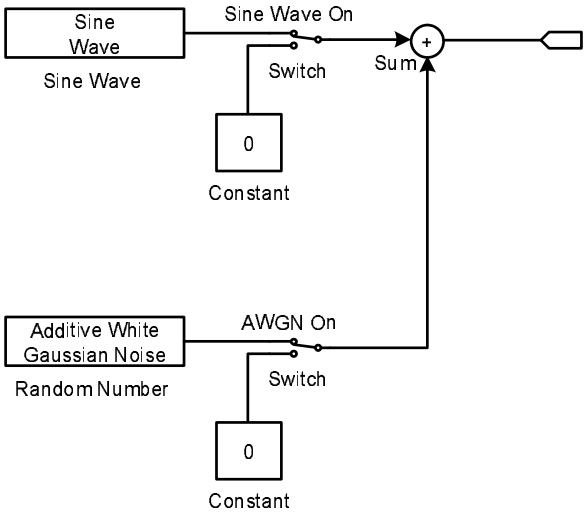


**Figure 3.20** Simunlink model: "Input Generator".

The "Input Generator" model is constructed by the "Sine Wave", "Random Number", "Sum", "Switch" and "Constant" blocks in Simulink, as shown in Fig. 3.20. This model collects all the voltage inputs used in the simulation, just for the convenience of the users. The parameters to setup in the model block dialog box are described in Table 3.8 and the input signals for different applications are summarized in Table 3.9. When operating in continuous mode, the "Sine Wave" block can become inaccurate due to loss of precision as time becomes very large. Here, we should set the sampling time is set as $1/(8 \times 10^6)$ in order to achieve adequate accuracy.

| **Parameters (Unit)** | **Descriptions (Values)** |
|---|---|
| $A$ (V) | Sine wave amplitude (0.594) |
| $f$ (Hz) | Sine wave frequency ($100 \times 10^3$) |
| $Var$ | AWGN variance (1) |
| $T_s$ (s) | Sampling time ($1/(8 \times 10^6)$) |
| Input Type | Sine wave, zero or AWGN |

**Table 3.8** Parameters to setup in "Input Generator".

| **Parameters (Input Signals)** | **Applications** |
|---|---|
| Sine Wave | Sensing output generation |
| Zero | Sensing noise test |
| AWGN | Transfer function generation |

**Table 3.9** Input signals for different applications.

## 3.2. Simulink Models for IS FEE PFM Actuation Hardware

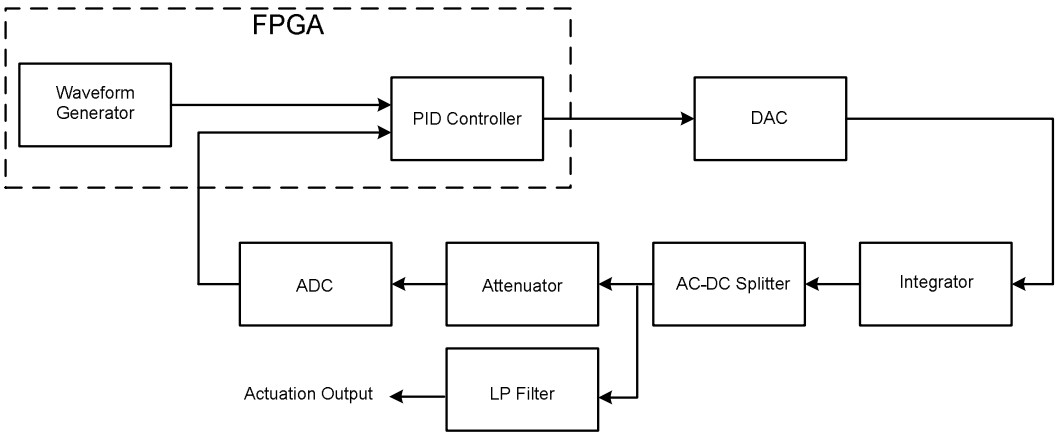


**Figure 3.21** Sigma-delta loop of the actuation.

The Simulink models of the PFM actuation hardware are mainly used for the simulation of the sigma-delta loop, and the simplified schematic of the sigma-delta loop is given in Fig. 3.21. The waveform generator generates the AC and DC actuation signal command as one input of the PID controller, the PID controller is used to minimize the error between the waveform generator output and the feedback ADC output, in order to provide stable actuation output. The waveform generator and PID controller are implemented on FPGA, the detail architectures of the FPGA are given in Appendix A.3. The digital-to-analog converter (DAC) convert the digital output of the PID controller to analog signal, and this analog signal is further processed by the integrator, AC-DC splitter and LP filter in order to provide the actuation output on the electrode. The output of the AC-DC splitter is also attenuated and converted to digital signal by the feedback ADC, which is the other input of the PID controller.

### 3.2.1. Waveform generator

The Waveform Generator models, including "Waveform Generator (16bit ADC)" and "Waveform Generator (24bit ADC)", are constructed by the "Digital Clock", "Constant", "Product", "Sine", "Sum", "Switch", "Gain", "Data Type Converter" and "CIC Interpolator" blocks in Simulink.

The block diagram of the "Waveform Generator (16bit ADC)" is shown in Fig. 3.22. This model is used in the sigma-delta loop with 16-bit ADC. The input commands, i.e. AC and DC amplitude commands, can be defined either in voltage or in bits, i.e. 16 bits or 20 bits. Both interpolated and non-interpolated output commands are provided, which are "INT Out" and "NON-INT Out", respectively. The output command formats of the blocks are given in the form of $< S, N, D >$, where $S$ denotes the number of bits for the sign, $N$ denotes the total number of bits, and $D$ denotes the number of bits for the decimal. Also, sampling time of the blocks is distinguished by different shadows, as shown in Fig. 3.22.

The parameters to setup in the model block dialog box are described in Table 3.10. The values of each parameter for the PFM hardware are also given in the table.

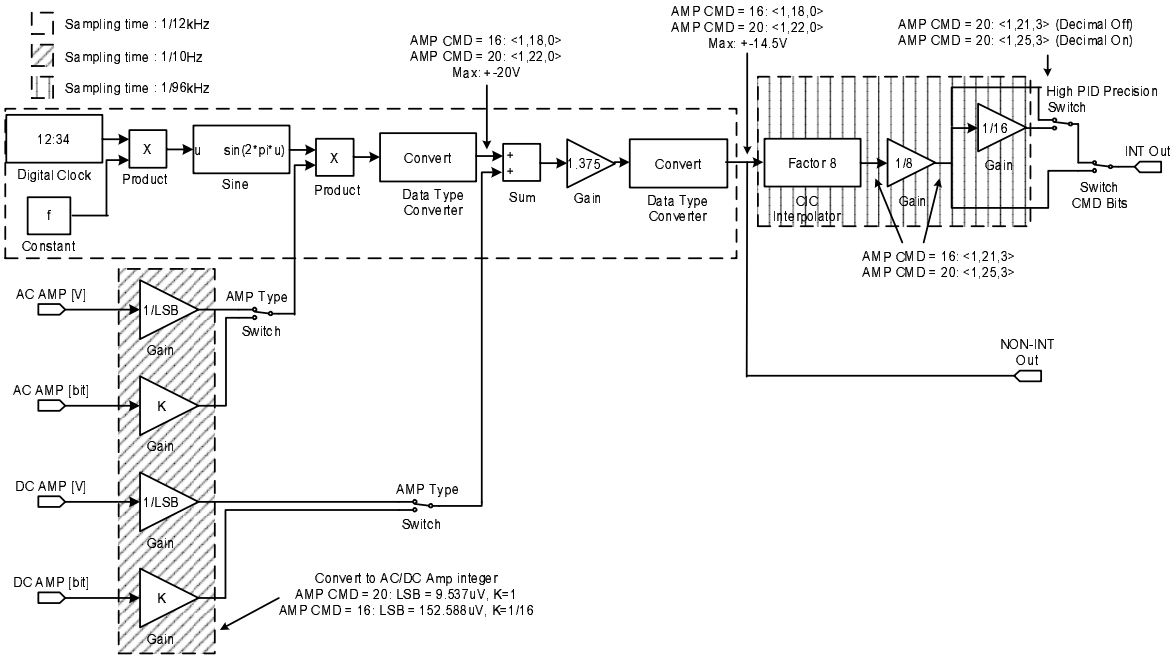


**Figure 3.22** Simunlink model: "Waveform Generator (16bit ADC)".

| Parameters (Unit) | Descriptions (Values) |
|---|---|
| $f$ (Hz) | Actuation waveform frequency |
| $T_s'$ (s) | Waveform tick sampling time ($1/(12 \times 10^3)$) |
| Amplitude Command Bits | The bits length of the waveform amplitude (16 or 20) |
| Amplitude Type | Generate the waveform in voltage or in bits |
| High PID Precision | PID controller running in high or low precision |

**Table 3.10** Parameters to setup in "Waveform Generator (16bit ADC)".

The PFM hardware uses 16 bits as the waveform amplitude, and here 20 bits waveform amplitude is also provided as an option to investigate benefit of better resolution. Also, note that the input command in bits, i.e., "AC AMP [bit]" and "DC AMP [bit]", should always be based on 20-bit resolution. When the amplitude command bits "AMP CMD" is chosen as 16, the input command is automatically converted to 16-bit resolution waveform amplitude integer number by multiplying the scale factor $K = 1/16$. The waveform amplitude integer number is then scaled by the factor 1.375, in order to make the best use of the dynamic range of the feedback ADC in the sigma-delta loop. The "INT Out" of the waveform generator provides interpolator output to the followed PID controller with command format $< 1, 21, 3 >$.

The GRS FEE use 20 bits as the waveform amplitude and different operations, as explained in Section A.3.2, can be defined by the "High PID Precision" switch. When this switch is off, the PID controller is running at low precision mode. The interpolator output is divided by 16 and the "INT Out" is truncated to 21-bit command with format of $< 1, 21, 3 >$, which is the data format of the PID controller input. When this switch is on, the PID controller is

running at high precision mode. The interpolator output is directly connected to the "INT Out" without extra operation, and thus "INT Out" has the command format $< 1, 25, 3 >$, which has better precision and requires the PID controller to run in higher precision mode. Note that the "High PID Precision" switch in the PID controller should be synchronized with the switch here.

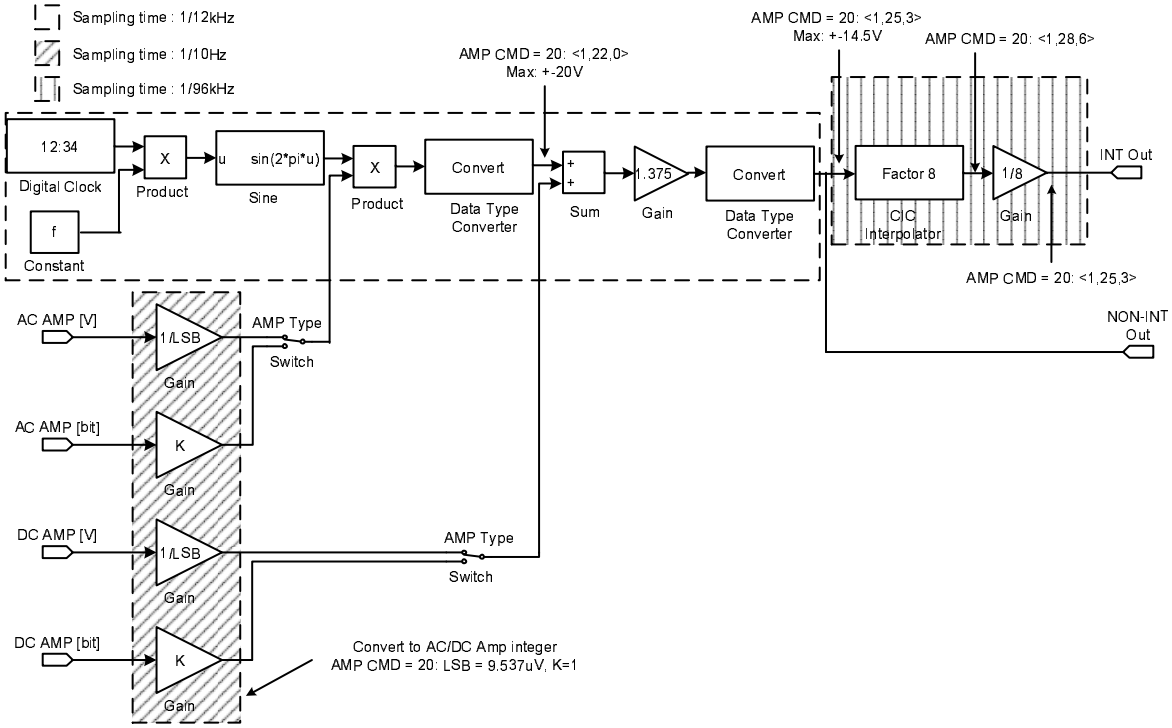


**Figure 3.23** Simunlink model: "Waveform Generator (24bit ADC)".

"Waveform Generator (24bit ADC)", as shown in Fig. 3.23, is used in the sigma-delta loop with 24-bit ADC and the input commands of 20 bits for the GRS FEE. The parameters to setup in the model block dialog box are described in Table 3.11. The values of each parameter are also given in the table. The PID controller for 24-bit ADC is always running at high precision, and thus there is no switch for it.

| Parameters (Unit) | Descriptions (Values) |
|---|---|
| $f$ (Hz) | Actuation waveform frequency |
| $T_s'$ (s) | Waveform tick sampling time ($1/(12 \times 10^3)$) |
| Amplitude Type | Generate the waveform in voltage or in bits |

**Table 3.11** Parameters to setup in "Waveform Generator (24bit ADC)".

### 3.2.2. PID controller

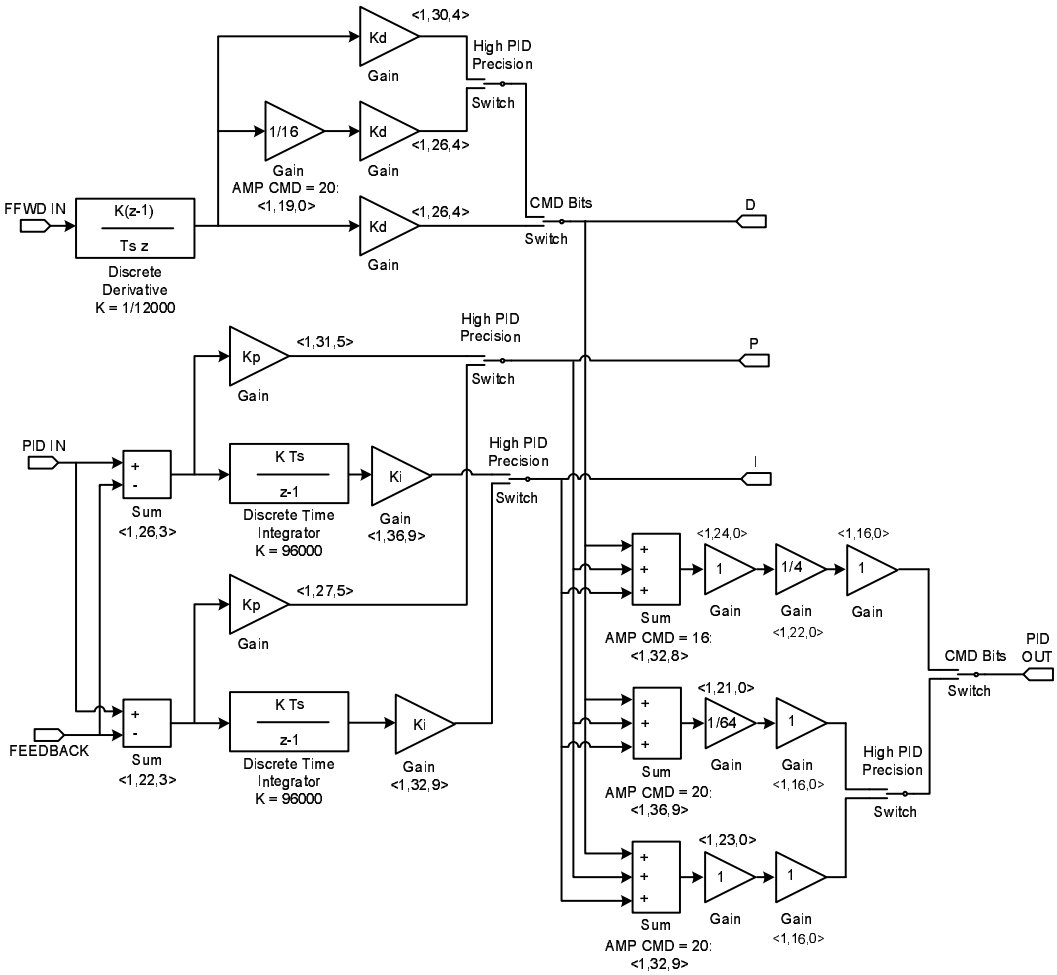


**Figure 3.24** Simunlink model: "PID Controller (16bit ADC)".

The PID Controller models, including "PID Controller (16bit ADC)" and "PID Controller (24bit ADC)", are constructed by the "Discrete Derivative", "Discrete Time Integrator", "Switch", "Sum" and "Gain" blocks in Simulink.

The block diagram of the "PID Controller (16bit ADC)" as shown in Fig. 3.24. This model is used in the sigma-delta loop with 16-bit ADC. The detail of the PID control can be found in [11]. Note that in the IS FEE, the derivation is applied on the feed forward input (FFWD IN) signal but not on the error signal as in the traditional PID control scheme. The inputs include the "FFWD IN", "PID IN" and "FEEDBACK". In the sigma-delta loop using 16-bit ADC, the "FEEDBACK" input is the ADC output adding extra zero value LSBs, in order to correctly calculated the error. The PID controller operation can be defined by the "CMD Bits" and "High PID Precision" switches, as shown in Table 3.12. The block diagram of different operations can be found in the Appendix A.3. The output signal formats of some blocks are also given in the form of $< S, N, D >$, as defined in Section 3.2.1. "PID OUT" is the PID controller output, and the "P", "I", "D" outputs are provided so that the PID

signals can be observed in the scope separately.

| CMD Bits | High PID Precision | PID Operation | Reference |
|---|---|---|---|
| 16-bit | OFF | 16-bit CMD with low PID precision | Fig. A.5 |
| 16-bit | ON | N/A | N/A |
| 20-bit | OFF | 20-bit CMD with low PID precision | Fig. A.6 |
| 20-bit | ON | 20-bit CMD with high PID precision | Fig. A.7 |

**Table 3.12** Definition of the PID controller operation.

The parameters to setup in the model block dialog box are described in Table 3.13. The values of each parameter for the PFM hardware are also given in the table.

| Parameters (Unit) | Descriptions (Values) |
|---|---|
| $K_p$ | Proportional gain (5.0625) |
| $K_d$ | Derivative gain (4) |
| $K_i$ | Integral gain (0.3281) |
| $T_s'$ (s) | Waveform tick sampling time ($1/(12 \times 10^3)$) |
| $T_s$ (s) | Sampling time ($1/(96 \times 10^3)$) |
| Amplitude Command Bits | The bits length of the waveform amplitude (16 or 20) |
| High PID Precision | PID controller running in high or low precision |

**Table 3.13** Parameters to setup in "PID Controller (16bit ADC)".

In the IS FEE, the ADC output has the signal format $< 1, 16, 0 >$, and extra LSBs with value 0 should be added to align the ADC output with the PID controller resolution, i.e. 2 for the low precision PID and 6 for the high precision PID. Then, the modified ADC output is provided to the "FEEDBACK" input of the PID controller. Here, 1 bit is added to the difference of the "PID IN" and "FEEDBACK" in order to prevent clipping. The summed PID signal is further scaled in order to provided the input for the forward 16-bit DAC.

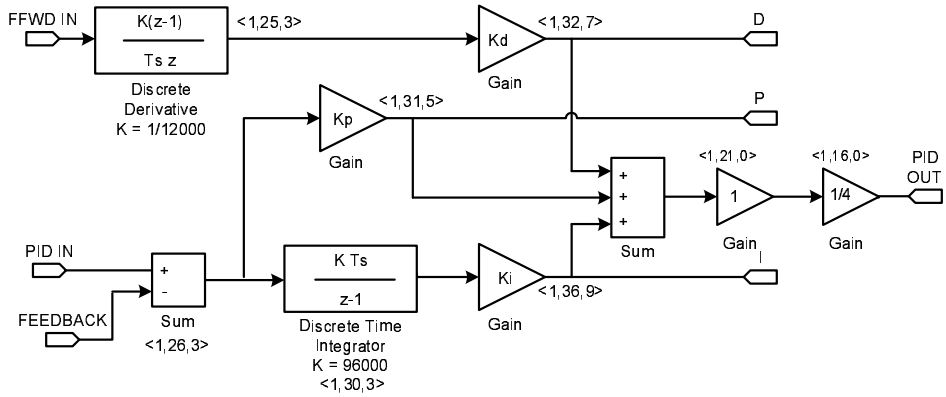


**Figure 3.25** Simunlink model: "PID Controller (24bit ADC)".

"PID Controller (24bit ADC)", as shown in Fig. 3.25, is used in the sigma-delta loop with 24-bit ADC and the input commands of 20 bits for the GRS FEE. The parameters to setup

in the model block dialog box are described in Table 3.14. The values of each parameter are also given in the table. The PID controller for 24-bit ADC is always running at high precision, and thus there is no switch for it.

| **Parameters (Unit)** | **Descriptions (Values)** |
|---|---|
| $K_p$ | Proportional gain (5.0625) |
| $K_d$ | Derivative gain (4) |
| $K_i$ | Integral gain (0.3281) |
| $T_s'$ (s) | Waveform tick sampling time ($1/(12 \times 10^3)$) |
| $T_s$ (s) | Sampling time ($1/(96 \times 10^3)$) |

**Table 3.14** Parameters to setup in "PID Controller (24bit ADC)".

In the GRS FEE, 24-bit ADC is recommended in the sigma-delta loop and the ADC output has the signal format $< 1, 24, 0 >$. The block diagram is given in Fig. A.8 in the Appendix A.3. Two LSBs should be removed to align the ADC output with the PID controller resolution. Then, the modified ADC output is provided to the "FEEDBACK" input of the PID controller. Also, 1 bit is added to the difference of the "PID IN" and "FEEDBACK" in order to prevent clipping. The summed PID signal is further scaled in order to provided the input for the forward 16-bit DAC.

### 3.2.3. ADC and DAC

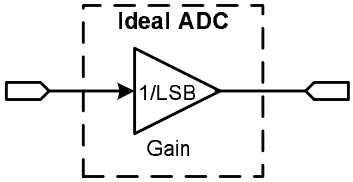


**Figure 3.26** Simunlink model: Ideal "ADC".

The ideal "ADC" model is constructed by the "Gain" block in Simulink, as shown in Fig. 3.26. These models are used to simulate ideal ADC. The "Gain" of the ADC is equivalent to the value of 1/LSB, and the LSB is defined similarly as

$$LSB = \frac{\tilde{V}_{max} - \tilde{V}_{min}}{2^N} \tag{3.74}$$

where $\tilde{V}_{max}$ and $\tilde{V}_{min}$ are the maximum and minimum input voltages, respectively.

The parameters to setup in the model block dialog box is described in Tables 3.15. The values of each parameter for the PFM hardware are also given in the table.

| Parameters (Unit) | Descriptions (Values) |
|---|---|
| $\tilde{V}_{max}$ (V) | Maximum input voltage (2.5) |
| $\tilde{V}_{min}$ (V) | Minimum input voltage ($-2.5$) |
| $N$ (Bits) | Word length (16) |
| $T_s$ (s) | Sampling time ($1/(96 \times 10^3)$) |

**Table 3.15** Parameters to setup in "ADC".

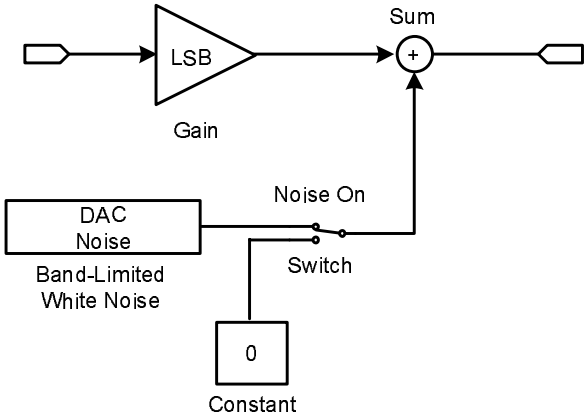


**Figure 3.27** Simunlink model: "DAC (+Noise)".

The "DAC (+Noise)" model is constructed by the "Gain", "Band-Limited White Noise", "Sum", "Switch" and "Constant" blocks in Simulink, as shown in Fig. 3.27. The "Gain" of

the DAC is equivalent to the value of the LSB, defined as

$$LSB = \frac{V_{max} - V_{min}}{2^N} \tag{3.75}$$

where $N$ is the word length, $V_{max}$ and $V_{min}$ are the maximum and minimum output voltages, respectively. This model is used to simulate DAC with output noise.

The parameters to setup in the model block dialog box are described in Tables 3.16. The values of each parameter for the PFM hardware are also given in the table.

| **Parameters (Unit)** | **Descriptions (Values)** |
|---|---|
| $V_{max}$ (V) | Maximum output voltage (4.5) |
| $V_{min}$ (V) | Minimum output voltage ($-4.5$) |
| $N$ (Bits) | Word length (16) |
| $T_s$ (s) | Sampling time ($1/(96 \times 10^3)$) |
| $Var$ ($V^2$) | Noise power ($2.4 \times 10^{-10}$) |
| Noise Switch On | Switch on or off the DAC noise |

**Table 3.16** Parameters to setup in "DAC (+Noise)".

### 3.2.4. Integrator

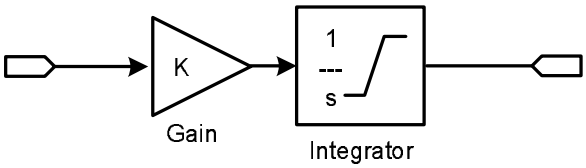


**Figure 3.28** Simunlink model: "Integrator".

The "Integrator" model is constructed by the "Gain" and "Integrator" blocks in Simulink, as shown in Fig. 3.28. This model is used to simulate the integrator connected to the output of the DAC in sigma-delta loop. The simplified circuit of the integrator is given in Fig. 3.29. The output voltage $V_o$ can be written as

$$V_o = \frac{1}{sRC}V_i = \frac{1}{RC}\frac{1}{s}V_i = \frac{1}{37.4k \times 10n}\frac{1}{s}V_i \approx 2674\frac{1}{s}V_i \tag{3.76}$$

where $V_i$ is the voltage input, $R$ and $C$ are resistor and capacitor as shown in Fig. 3.29. The output of the integrator is limited by the integrator upper and lower bounds, which are equivalent to the OpAmp supply voltages in the real circuit.

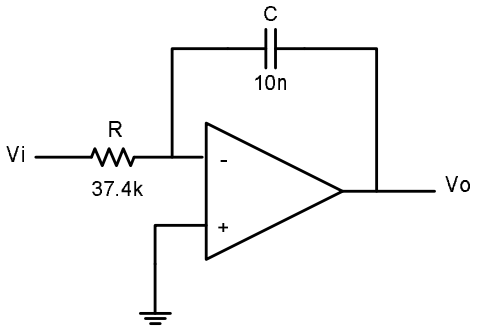


**Figure 3.29** Integrator circuit.

The parameters to setup in the model block dialog box are described in Table 3.17. The values of each parameter for the PFM hardware are also given in the table.

| Parameters (Unit) | Descriptions (Values) |
|---|---|
| $K$ | Integrator gain (2674) |
| Integrator upper bound (V) | OpAmp supply voltage (14.5) |
| Integrator lower bound (V) | OpAmp supply voltage ($-14.5$) |

**Table 3.17** Parameters to setup in "Integrator".

### 3.2.5. AC-DC splitter and output filter

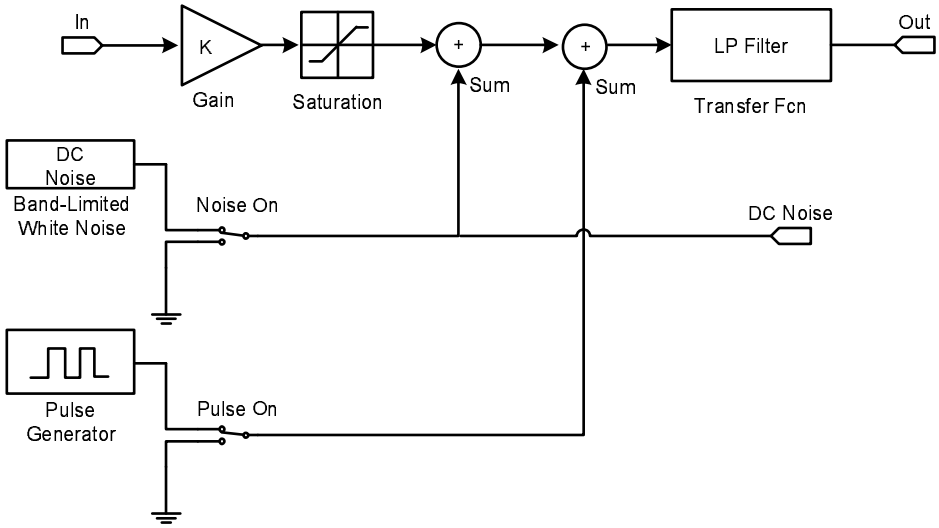


**Figure 3.30** Simunlink model: "AC-DC Splitter".

The simple "AC-DC Splitter" model is constructed by the "Gain", "Saturation", "Transfer Fcn", "Band-Limited White Noise", "Pulse Generator", "Sum" and "Swtich" blocks in Simulink, as shown in Fig. 3.30. This model is used to simulate the AC-DC splitter following the integrator in sigma-delta loop. The circuit of the AC-DC splitter is given in Fig. 3.31.

The AC-DC splitter can be simplified to the circuit shown in Fig. 3.32. The intermediate signal $V_m'$ can be approximate by

$$V_m' = \frac{R5}{R1}V_i = \frac{663k}{412k}V_i \approx 1.6092V_i \tag{3.77}$$

where $R1$ and $R5$ are the resistors as shown in Fig. 3.32. The output of the AC-DC splitter is limited by the upper and lower bounds for approximately $\pm$14.5V as given in Table. 3.18, which is equivalent to the OpAmp supply voltage. The supply voltage is $\pm$15V, but it is limited by the transistor driver to about $\pm$14.5V. The intermediate signal $V_m'$ is further filtered by a LP filter with corner frequency $3.9k$Hz, since the bandwidth of the feedback loop is about $3.9k$Hz. The output of the AC-DC splitter $V_o$ can be written as

$$V_o = \frac{1}{s\tau + 1}V_m = \frac{1}{sR_6C_6 + 1}V_m = \frac{1}{(1/3.9k/2\pi)s + 1}V_m = \frac{1}{4.083 \times 10^{-5}s + 1}V_m. \tag{3.78}$$

Here, $R_6$ and $C_6$ are used to model the time constant $\tau$, which is decided by the bandwidth of the feedback loop $3.9k$Hz.

The analog noise in this model is simulated by the output DC noise measured in the hardware. The DC noise density is $3.23\mu V/\sqrt{Hz}$ for $f >$ 1Hz and the $1/f$ noise under 1Hz is not modeled here. The noise power of the "Band-Limited White Noise" block is defined as $P_{dc} \times T_s$, where $P_{dc}$ is the square of the root mean square (RMS) value of the DC voltage noise, i.e., $V_{rms}^2$, and $T_s$ is the sampling time of the noise. The noise sampling frequency $1/T_s$ should be at least 16 times, i.e., $100/2\pi$, larger than the signal bandwidth, which is minimum $16 \times 4.8k = 77k$Hz. For $T_s = 1/96k$, the $V_{rms} = 1m$V and $P_{dc}$ is then $10^{-6}V^2$.

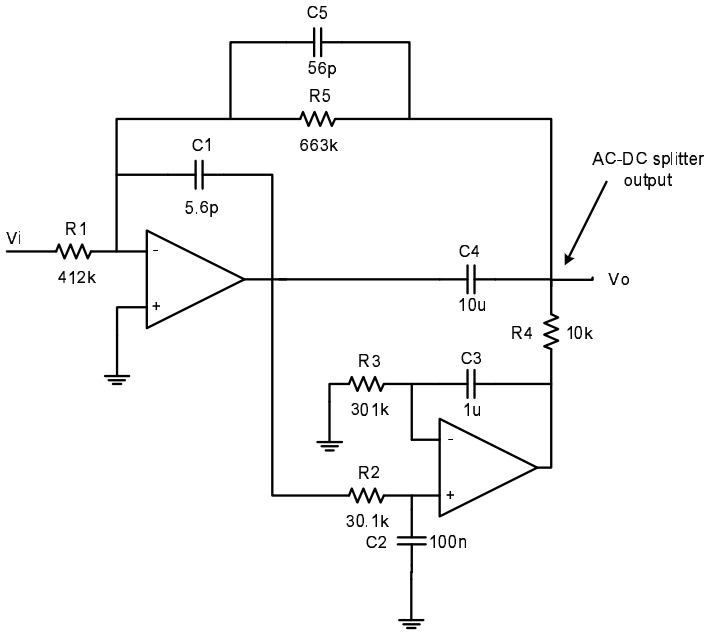


**Figure 3.31** AC-DC splitter circuit.

Since some unexpected pulses are observed at the electrode in the real hardware measurement, the pulse generator is used here in order to investigate whether the source of the unexpected pulses is in the AC-DC splitter.

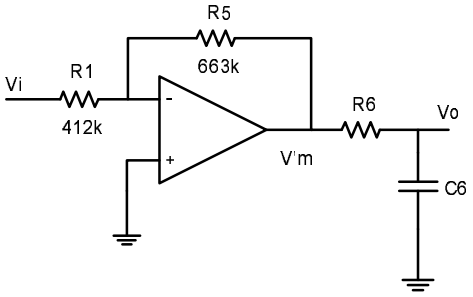


**Figure 3.32** Simplified AC-DC splitter circuit.

The parameters to setup in the model block dialog box are described in Table 3.18. The values of each parameter for the PFM hardware are also given in the table.

The "Output Filter" model is constructed by the "Transfer Fcn" blocks in Simulink, as shown in Fig. 3.33. This model is used to simulate the followed LP filters at the output of the AC-DC splitter, in order to provide actuation output on the electrodes. The circuit of the output filter is given in Fig. 3.34.

| Panels | Parameters (Unit) | Descriptions (Values) |
|---|---|---|
| AC-DC | $K$ | AC-DC splitter DC gain (1.6092) |
| Splitter | Voltage upper bound (V) | Limited OpAmp supply voltage (14.5) |
| | Voltage lower bound (V) | Limited OpAmp supply voltage ($-14.5$) |
| | $P_{dc}$ ($V^2$) | DC noise power ($10^{-6}$) |
| | $T_s$ (s) | Noise sampling time ($1/(96 \times 10^3)$) |
| | DC Noise Switch | Switch on or off the DC noise |
| Pulse | $A$ (V) | Amplitude of the pulse ($50 \times 10^{-6}$) |
| Generator | $T_p$ (s) | Period of the pulse (1) |
| | $W$ (% of the period) | Width of the pulse (50) |
| | $\tau$ (s) | Delay of the pulse (0.5) |
| | Pulse Switch | Switch on or off the pulse |

**Table 3.18** Parameters to setup in "AC-DC Splitter".

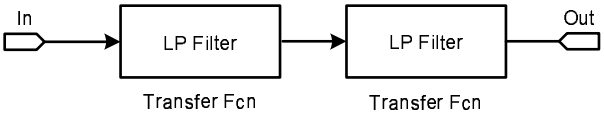


**Figure 3.33** Simunlink model: "Output Filter".

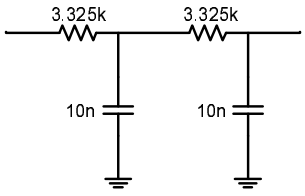


**Figure 3.34** Output filter circuit.

### 3.2.6. Attenuator and other blocks

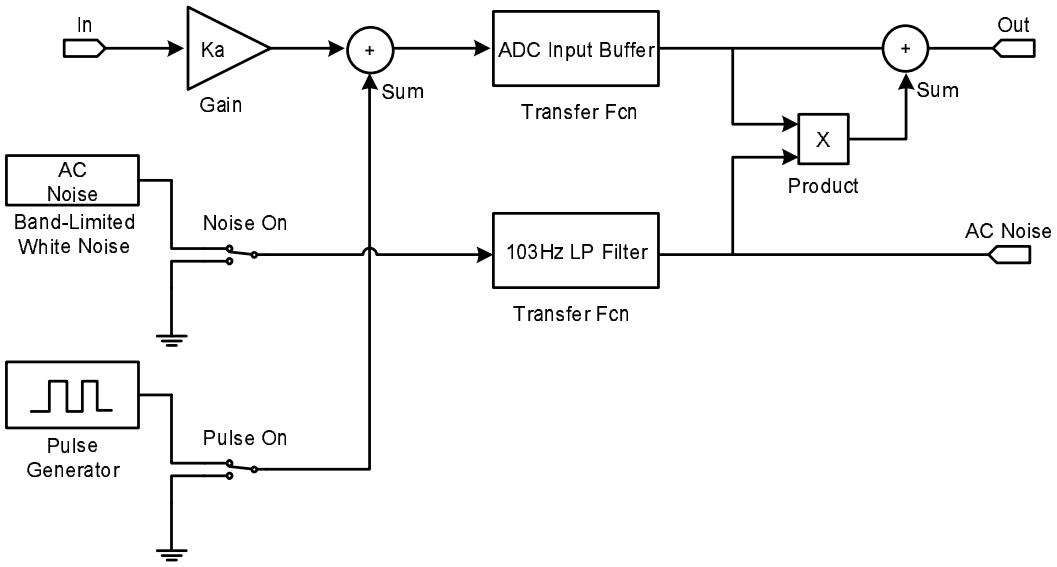


**Figure 3.35** Simunlink model: "Attenuator".

The "Attenuator" model is constructed by the "Gain", "Transfer Fcn", "Band-Limited White Noise", "Product", "Pulse Generator", "Sum" and "Switch" blocks in Simulink, as shown in Fig. 3.35. This model is used to simulate the attenuator preceding the ADC in sigma-delta loop. The circuit of the attenuator is given in Fig. 3.36 and the output of the attenuator $V_o$ can be written as

$$\begin{aligned} V_o &= \frac{1}{sR_2C_1+1}\frac{R_2}{R_1}V_i = \frac{1}{s16.98k \times 464p + 1}\frac{16.98k}{102k}V_i \\ &\approx \frac{1}{7.879 \times 10^{-6}s + 1}0.1665V_i. \end{aligned} \tag{3.79}$$

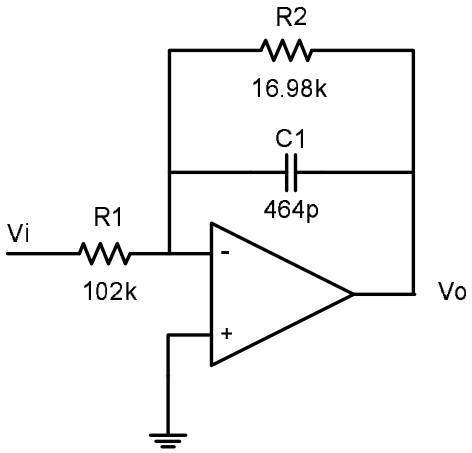


**Figure 3.36** Attenuator circuit.

To simulate the multiplicative AC noise - actuation amplitude instability, we multiply the ADC input with the noise expressed in *ppm* and add to the input, which will be equivalent to the ADC voltage reference fluctuation. The maximum AC noise density measured on hardware is $3ppm/\sqrt{Hz}$ (1.5 factor violation at $1m$Hz), i.e., $3\mu V/\sqrt{Hz}$ for $1V$. Here the power of the "Band-Limited White Noise" block is defined as $(V_{rms}/10^6 \times A)^2 \times T_s'$, where $V_{rms}$ is the RMS value of the AC voltage noise in ppm, $A$ is the AC input amplitude and $T_s$ is the noise sampling time. Here, the noise sampling frequency $1/T_s$ is selected here to be $12k$Hz, i.e. well above the voltage reference bandwidth of 100Hz. Hence, the $3ppm/\sqrt{Hz}$ density is equivalent to $329ppm$ in $12k$Hz bandwidth. Note that the AC noise is only used when the ideal ADC model without noise is used in the simulation. In case the noise is simulated in the ADC block, i.e. "ADC (+Noise)" in Section 3.1.4 is used in the simulation, it should be turned off.

The pulse generator is used to investigate the reason of unexpected voltage jumps at certain electrodes in the real hardware measurement.

The parameters to setup in the model block dialog box are described in Table 3.19. The values of each parameter for the PFM hardware are also given in the table. Note that the attenuation gain $K_a$ is supposed to be $16.98/102 = 0.1665$. However, the attenuation gain is mainly based on the actuation output to ADC output range adjustment of $2.5V/15.02V$. Therefore, in our model we use $2.5V/14.545V = 0.17188$ instead to prevent systematic error in the output.

| **Pannels** | **Parameters (Unit)** | **Descriptions (Values)** |
|---|---|---|
| Attenuator | $K_a$ | Attenuator gain (0.171875) |
| | $V_{rms}$ (ppm) | RMS value of the AC noise in ppm (329) |
| | $A$ | AC amplitude (1) |
| | $T_s$ (s) | Noise sampling time ($1/(12 \times 10^3)$) |
| | AC Noise Switch | Switch on or off the AC noise |
| Pulse | $A$ (V) | Amplitude of the pulse ($50 \times 10^{-6}$) |
| Generator | $T_p$ (s) | Period of the pulse (1) |
| | $W$ (% of the period) | Width of the pulse (50) |
| | $\tau$ (s) | Delay of the pulse (0.5) |
| | Pulse Switch | Switch on or off the pulse |

**Table 3.19** Parameters to setup in "Attenuator".

There are two additional models in the library for noise calculation and output measurement, and the detail of these models can be seen by double clicking the model blocks. These models are used in the next chapter in order to calculate the AC and DC noises, and measure the DC and peak values of the electrode voltage, see Section 5.3

Chapter 4

# Further Simplified Models for the Hardware

In this chapter, the models in the "Simulink Library" are further simplified in order to simulate even longer time period, e.g., simulation of 1 hour.

## 4.1. Simplified Models for IS FEE PFM Sensing Hardware

In the sensing hardware, the output of the transformer, transimpedance amplifiers (TIAs) and differential amplifier is an amplitude modulation (AM) signal and the carrier is $100k$Hz sine wave. This AM signal will be filtered by the band pass (BP) filter with central frequency $100k$Hz, in order to magnify the in-band signal around $100k$Hz and reduce the out-of-band noise. The output of the BP filter will be demodulated in order to extract the amplitude of the modulating signal, which represents the sensing signal, from the carrier wave. For further simplified models, we only need to consider the in-band signal processing around $100k$Hz and ignore the out-of-band behavior of the hardware. The modeling of different parts of the sensing hardware is introduced in the following sections.

### 4.1.1. Transformer, TIAs and differential amplifier

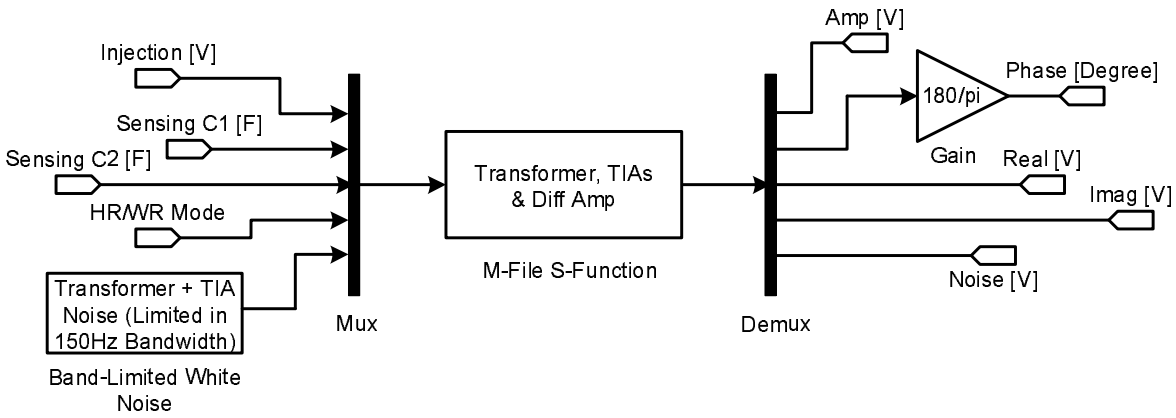


**Figure 4.1** Simplified model: "Transformer+TIAs+Diff Amp (M-File S-Function)".

The "Transformer+TIAs+Diff Amp (M-File S-Function)" model is constructed by the "S-Function", "Band-Limited White Noise", "Gain", "Mux" and "Demux" blocks in Simulink, as shown in Fig. 4.1. This model is used to simulate the in-band system behavior at $100k$Hz, and the parameters to setup in the model block dialog box are described in Table 4.1. The values of each parameter for the PFM hardware are also given in the table. Note that the parameters of the operational amplifier (OpAmp) used in the model is from the parameters of "OP467" [5], and the parameters of the junction gate field-effect transistor (JFET) used in the model is from the parameters of "2N4393" [7]. Also note that the TIA input capacitance should be equal to the input capacitance of "2N4393".

| **Panels** | **Parameters (Unit)** | **Descriptions (Values)** |
|---|---|---|
| Transformer | $L_1$, $L_2$, $L_3$ (H) | Coil inductance ($4.2 \times 10^{-3}$) |
| | $C_{p1}$, $C_{p2}$ (F) | Resonance tuning capacitance ($310 \times 10^{-12}$) |
| | $C_{a1}$, $C_{a2}$ (F) | Actuation capacitance ($10 \times 10^{-9}$) |
| | $K$ | Coupling coefficient (1) |
| | $Q$ | Quality factor (200) |
| TIAs | $C_{d1}$, $C_{d2}$ (F) | Decoupling capacitance ($10 \times 10^{-9}$) |
| | $A_{ov}$ (dB) | OpAmp large signal voltage gain (80) |
| | $f_c$ (Hz) | Corner frequency of $A_{ov}$ ($4 \times 10^3$) |
| | $C_i$ (F) | TIA Input capacitance ($14 \times 10^{-12}$) |
| | $D_{v1}$ (V/sqrt(Hz)) | OpAmp voltage noise density ($7 \times 10^{-9}$) |
| | $D_{v2}$ (V/sqrt(Hz)) | JFET voltage noise desnity ($3 \times 10^{-9}$) |
| | $D_i$ (A/sqrt(Hz)) | JFET gate current noise density ($2.5 \times 10^{-15}$) |
| | $R_f$ (Ohm) | Feedback resistance ($5.6 \times 10^6$) |
| | $C_f$ (F) | Feedback capacitance ($3.3 \times 10^{-12}$) |
| Differential Amplifier | $R_1$, $R_2$, $R_3$ (Ohm) | Resistance (976, 944, $18.7 \times 10^3$) |
| | $C_3$ (F) | Decoupling capacitance($10 \times 10^{-9}$) |
| | $C_4$ (F) | Capacitance ($100 \times 10^{-12}$) |
| Others | $T$ (Kelvin) | Temperature (300) |
| | $T_s$ (s) | Sampling time (1/20) |

**Table 4.1** Parameters to setup in "Transformer+TIAs+Diff Amp (M-File S-Function)".

### M-File S-Function model

The "S-Function" block is used to model the in-band system behavior at $100k$Hz. The "S-Function" has five input arguments, which are the injection voltage input $V_i$, the sensing capacitance $C_1$ and $C_2$, the HR/WR mode switch, and the noise input $n_i$. The parameters of the "S-Function" include the parameters of the transformer, TIA and differential amplifier etc. The behavior of the "S-Function" is written in M file using M-File S-Function. The output of the transformer and TIAs $V_o'$ is calculated by

$$V_o' = H_1(s)V_i|_{s=j\omega_0} = H_1(s)V_i|_{s=j2\pi 100k} \tag{4.1}$$

where $H_1(s)$ is the transfer function of the transformer and TIAs defined as in (3.18) in Section 3.1.1, and $\omega_0 = 2\pi 100k$. The voltage output of the differential amplifier $V_o$ is calculated by

$$V_o = H_2(s)V_o'|_{s=j\omega_0} = H_2(s)V_o'|_{s=j2\pi 100k} \tag{4.2}$$

where $H_2(s)$ is the transfer function of the differential amplifier defined as in (3.23) for HR mode and (3.24) for WR mode in Section 3.1.1. From above equations, we can see that the voltage output $V_o$ should be a complex signal. However, the M-File S-Function does not support complex output. Hence we provide the voltage output as an output group containing amplitude and phase, as well as real and imagine part.

The noise output $n_o$ is calculated by

$$n_o = |H_2(s)|n_i|_{s=j\omega_0} = |H_2(s)|n_i|_{s=j2\pi 100k} \tag{4.3}$$

where the noise input $n_i$ is a band limited white noise. The bandwidth of the noise is limited to 150Hz and the power spectral density (PSD) of the noise $S'$ is defined as

$$S' = S'_{Z'_{eq}} + S'_{v+} + S'_{v-} + S'_i + S'_{Z_f}|_{f=100k}. \tag{4.4}$$

Here, $S'_{Z'_{eq}}$, $S'_{v+}$, $S'_{v-}$, $S'_i$ and $S'_{Z_f}$ are PSDs for different noise sources defined as in (3.37), (3.40), (3.41) and (3.42) in Section 3.1.1, respectively.

### C S-Function model

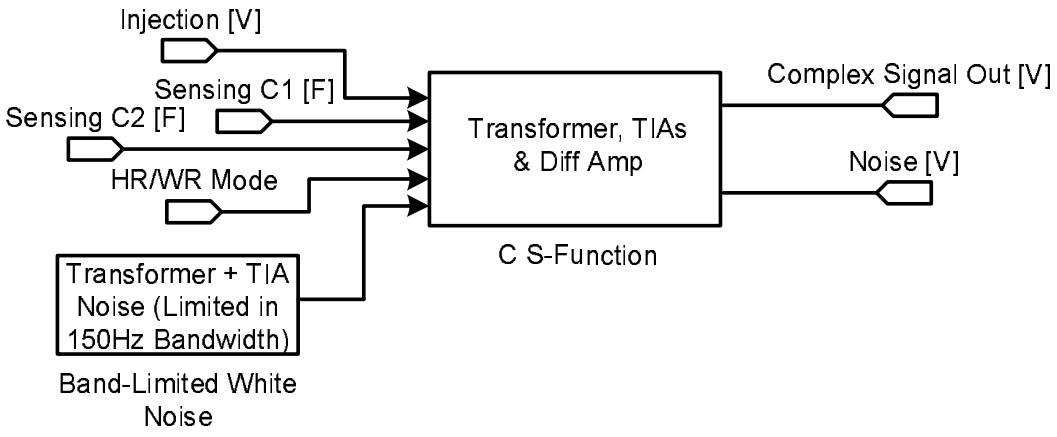


**Figure 4.2** Simplified model: "Transformer+TIAs+Diff Amp (C S-Function)".

In addition, the "Transformer+TIAs+Diff Amp (C S-Function)" model is provided as shown in Fig. 4.2. The function of this model is equivalent to the "Transformer+TIAs+Diff Amp (M-File S-Function)" and the parameters to setup in the model block dialog box are the same as in Table 4.1. The block is written in C file using C S-Function, which supports complex input and output. Also, the simulation using C S-Function is faster than the simulation using M-File S-Function.

### Transformer, TIAs and differential amplifier with cross talk

The actuation to sensing cross talk is very probably caused by the variation of the actuation capacitors due to the DC bias, typically when the capacitor is multilayer ceramic type [12]. Therefore, the M-File S-Function model and the C S-Function model are also slightly modified to demonstrate the actuation to sensing cross talk.

Two extra inputs $V_{act1}$ and $V_{act2}$ are added to the models. In the LTP, the actuation input is the sum of a AC signal and a DC signal. Based on our investigation, the cross talk is proportional to the peak values of the actuation inputs. Therefore, the values of $V_{act1}$ and $V_{act2}$ should be defined as the peak value of the actuation input.

An extra parameter needs to be defined in the model block dialog box, which is the actuation capacitor changing rate $K_c$ with unit $F/V$. Therefore, the real time values of the actuation capacitors in the models become

$$\begin{aligned} C_{a1} &= C_{a1} + K_c V_{act1} \\ C_{a2} &= C_{a2} + K_c V_{act2}. \end{aligned} \tag{4.5}$$

The demonstration of the actuation to sensing cross talk will be given in Chapter 5.

### 4.1.2. Bandpass filter

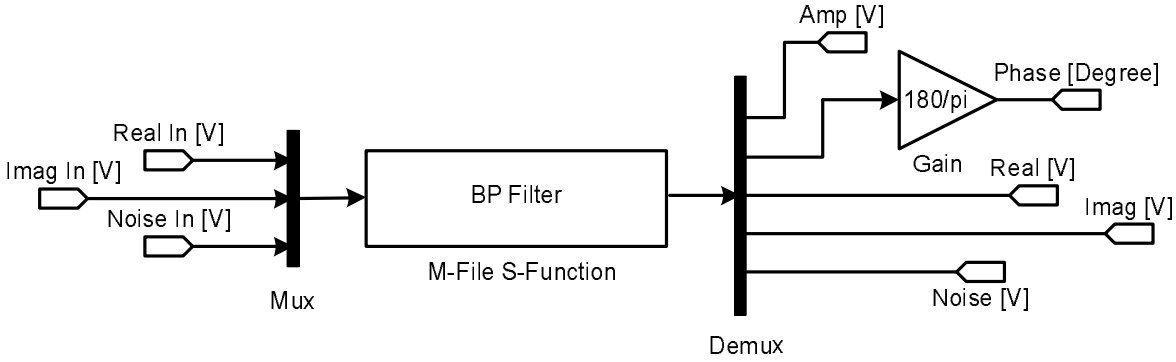


**Figure 4.3** Simplified model: "Band Pass Filter (M-File S-Function)".

The "Band Pass Filter (M-File S-Function)" model is constructed by the "S-Function", "Gain", "Mux" and "Demux" blocks in Simulink, as shown in Fig. 4.3. This model is used to simulate the in-band system behavior at $100k$Hz, consisting of a high pass (HP) filter followed by a low pass (LP) filter and a gain compensation. The gain compensation is used to compensate the output voltage amplitude level, in order to achieve the same voltage output amplitude as the real PFM hardware. There is no noise source in the model, since the noise is negligible compared to the noise from the transformer and TIAs. The parameters to setup in the model block dialog box are described in Table 4.2. The values of each parameter for the PFM hardware are also given in the table.

| Panels | Parameters (Unit) | Descriptions (Values) |
|---|---|---|
| HP Filter | $R_1$, $R_2$, $R_3$ (Ohm) | Resistance ($22.6 \times 10^3$, $71.5 \times 10^3$, 178) |
| | $C_1$, $C_2$ (F) | Capacitance ($10^{-9}$) |
| LP Filter | $R_1$ to $R_5$ (Ohm) | Resistance ($3.16 \times 10^3$, $11.5 \times 10^3$, 976, $93.1 \times 10^3$, $11.5 \times 10^3$) |
| | $C_1$, $C_2$, $C_3$ (F) | Capacitance ($10 \times 10^{-12}$, $10 \times 10^{-12}$, $10 \times 10^{-9}$) |
| Others | Gain Compensation | Compensate the gain of the BP Filter (1.0087) |
| | $T_s$ (s) | Sampling time (1/20) |

**Table 4.2** Parameters to setup in "Band Pass Filter (M-File S-Function)".

#### M-File S-Function

The "S-Function" block is used to model the in-band system behavior at $100k$Hz. The "S-Function" has three input arguments, which are the real input $v_r$, imaginary input $v_j$, and the noise input $n_i$. These inputs are connected to the real, imag and noise outputs of the "Transformer+TIAs+Diff Amp (M-File S-Function)" model in the simulation. The parameters of the "S-Function" include the parameters of the BP filter, and the behavior of the "S-Function" is written in M file using M-File S-Function. The output of the filter $V_o$ is calculated by

$$V_o = KH_3(s)H_4(s)(v_r + jv_j)|_{s=j\omega_0} = KH_3(s)H_4(s)(v_r + jv_j)|_{s=j2\pi 100k} \tag{4.6}$$

where $K$ is the compensation gain, $H_3(s)$ and $H_4(s)$ are the transfer functions of the HP filter and LP filter, defined as in (3.45) and (3.46) in Section 3.1.2, respectively.

The noise output $n_o$ is calculated by

$$n_o = K|H_3(s)H_4(s)|n_i|_{s=j\omega_0} = K|H_3(s)H_4(s)|n_i|_{s=j2\pi 100k}. \tag{4.7}$$

### C S-Function

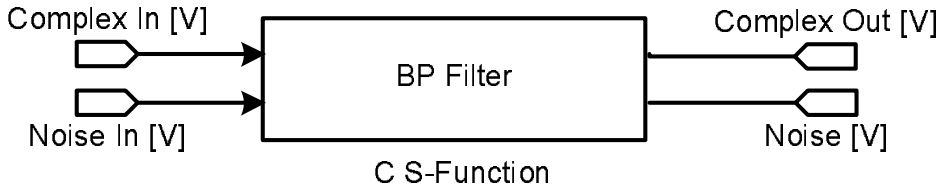


**Figure 4.4** Simplified model: "Band Pass Filter (C S-Function)".

In addition, the "Band Pass Filter (C S-Function)" model is provided as shown in Fig. 4.4. The function of this model is equivalent to the "Band Pass Filter (M-File S-Function)" and the parameters to setup in the model block dialog box are the same as in Table 4.2. The block is written in C file using C S-Function, which supports complex input and output. The complex input is connected to the complex output of the "Transformer+TIAs+Diff Amp (C S-Function)" model in the simulation. Also, the simulation using C S-Function is faster than the simulation using M-File S-Function.

### 4.1.3. Demodulator

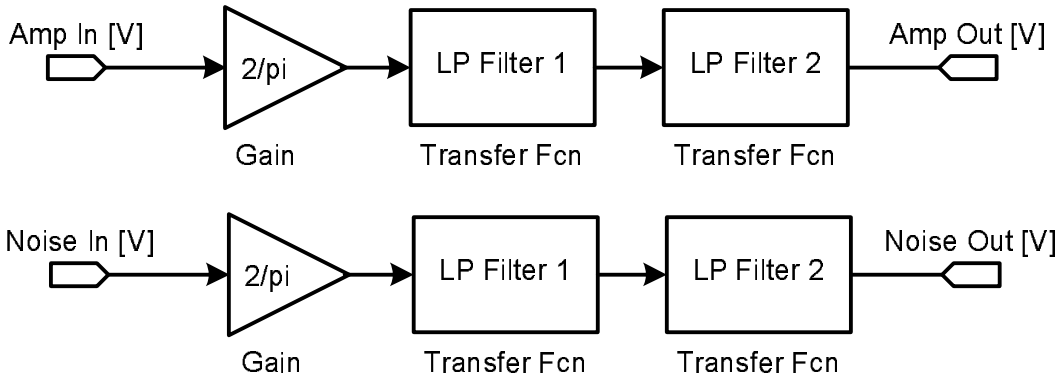


**Figure 4.5** Simplified model: "Demodulator".

The simplified "Demodulator" model is constructed by the "Transfer Fcn" and "Gain" blocks in Simulink, as shown in Fig. 4.5. Since we only consider the system behavior at $100k$Hz, the demodulation operation is simplified to a gain stage with value $2/\pi$. Note that the input of the model should be the signal amplitude, i.e., the output of the "Band Pass Filter (M-File S-Function)" model or the amplitude of the complex output of the "Band Pass Filter (C S-Function)" model.

The parameters to setup in the model block dialog box are described in Table 4.3. The values of each parameter for the PFM hardware are also given in the table.

| Panels | Parameters (Unit) | Descriptions (Values) |
|---|---|---|
| LP Filter 1 | $R_1$ (Ohm) | Resistance ($3.24 \times 10^3$) |
| | $C_1$ (F) | Capacitance ($330 \times 10^{-9}$) |
| LP Filter 2 | $R_2$, $R_3$ (Ohm) | Resistance ($3.24 \times 10^3$) |
| | $C_2$, $C_3$ (F) | Capacitance ($330 \times 10^{-9}$) |

**Table 4.3** Parameters to setup in "Demodulator".

#### Mode description

The output $V_o$ and noise output $n_o$ are calculated by

$$\begin{aligned} V_o &= \frac{2}{\pi}\left(\frac{1}{sR_1C_1+1}\right)\left(\frac{1}{s^2R_2R_3C_2C_3+sC_3(R_2+R_3)+1}\right)V_i|_{s=j2\pi 100k} \\ n_o &= \frac{2}{\pi}\left(\frac{1}{sR_1C_1+1}\right)\left(\frac{1}{s^2R_2R_3C_2C_3+sC_3(R_2+R_3)+1}\right)n_i|_{s=j2\pi 100k} \end{aligned} \tag{4.8}$$

where $V_i$ and $n_i$ are the amplitude and noise input, respectively.

## 4.2. Simplified Models for IS FEE PFM Actuation Hardware

Compared to the actuation models in the "Simulink Library", the detail of the sigma-delta loop is neglected for simplicity.

### 4.2.1. Actuation input

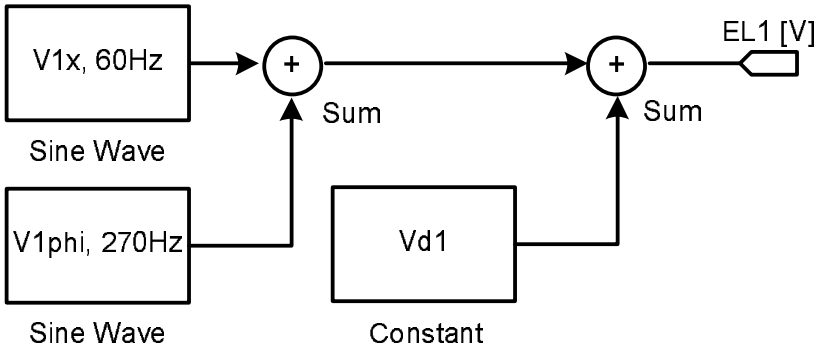


**Figure 4.6** Simplified model: "Actuation Input" on EL1.

The "Actuation Input ELx to ELy" model is simply constructed by the "Sine Wave", "Constant" and "Sum" blocks in Simulink. Fig. 4.6 gives an example of the actuation input on Electrode 1 (EL1). The actuation inputs on each EL are given as follows:

$$\begin{aligned} EL1 &= +V_{1x}sin(2\pi 60t) + V_{1\varphi}sin(2\pi 270t) + V_{d1} \\ EL2 &= -V_{1x}sin(2\pi 60t) + V_{2\varphi}cos(2\pi 270t) + V_{d2} \\ EL3 &= +V_{2x}cos(2\pi 60t) - V_{1\varphi}sin(2\pi 270t) + V_{d3} \\ EL4 &= -V_{2x}cos(2\pi 60t) - V_{2\varphi}cos(2\pi 270t) + V_{d4} \end{aligned} \tag{4.9}$$

$$\begin{aligned} EL5 &= +V_{1y}sin(2\pi 90t) + V_{1\theta}sin(2\pi 240t) + V_{d5} \\ EL6 &= -V_{1y}sin(2\pi 90t) + V_{2\theta}cos(2\pi 240t) + V_{d6} \\ EL7 &= +V_{2y}cos(2\pi 90t) - V_{1\theta}sin(2\pi 240t) + V_{d7} \\ EL8 &= -V_{2y}cos(2\pi 90t) - V_{2\theta}cos(2\pi 240t) + V_{d8} \end{aligned} \tag{4.10}$$

$$\begin{aligned} EL9 &= +V_{1z}sin(2\pi 90t) + V_{1\eta}sin(2\pi 240t) + V_{d9} \\ EL10 &= -V_{1z}sin(2\pi 90t) + V_{2\eta}cos(2\pi 240t) + V_{d10} \\ EL11 &= +V_{2z}cos(2\pi 90t) - V_{1\eta}sin(2\pi 240t) + V_{d11} \\ EL12 &= -V_{2z}cos(2\pi 90t) - V_{2\eta}cos(2\pi 240t) + V_{d12}. \end{aligned} \tag{4.11}$$

Here, $V_{ix}, V_{iy}$ and $V_{iz}, i = 1, 2$ are the amplitudes of the AC actuation waveform along axis $x, y$ and $z$, respectively. $V_{i\varphi}, V_{i\theta}$ and $V_{i\eta}, i = 1, 2$ are the amplitudes of the AC actuation waveform along torque $\varphi, \theta$ and $\eta$, respectively. $V_{di}, i = 1, ..., 12$ are the amplitudes of the DC actuation waveform. These parameters can be setup in the model block dialog box.

### 4.2.2. Flicker noise generator

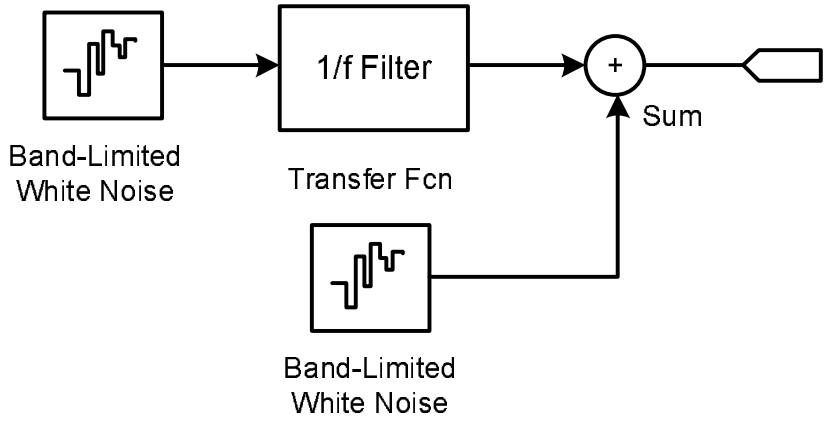


**Figure 4.7** Simplified model: "Noise Generator (+ 1/f Noise)".

The "Noise Generator (+ 1/f Noise)" model is constructed by the "Band-Limited White Noise", "Transfer Fcn", "Sum" and "Gain" blocks in Simulink, as shown in Fig. 4.7. The output of this model contains white noise and $1/f$ noise, and the $1/f$ noise is generated by a band-limited white noise filtered by the $1/f$ filter.

The parameters to setup in the model block dialog box are described in Table 4.4. The values of each parameter for the PFM hardware are also given in the table. The sampling time should be selected carefully, and the recommended value for the sampling time is $T_s < 1/(5 \times f_0 \times 10^{fdec})$.

| Parameters (Unit) | Descriptions (Values) |
|---|---|
| $f_0$ (Hz) | Lowest interested frequency for the $1/f$ filter ($1 \times 10^{-5}$) |
| $fdec$ (Decade) | Bandwidth of the $1/f$ filter from $f_0$ in decade (5) |
| $K$ (V/sqrt(Hz)) | Noise level at 1 Hz ($1 \times 10^{-6}$) |
| $A_w$ (F) | White noise ASD of the 1/f noise ($3.16 \times 10^{-6}$) |
| $T_s$ (s) | Sampling time (1/10) |

**Table 4.4** Parameters to setup in "Noise Generator (+ 1/f Noise)".

#### $1/f$ filter mode description

The initial transfer function of the $1/f$ filter is defined as

$$\tilde{H}_{1/f}(s) = \frac{(s - z_0)(s - z_1)...(s - z_{fdec-2})}{(s - p_0)(s - p_1)...(s - p_{fdec-1})} \tag{4.12}$$

where $fdec$ is the interested bandwidth of the $1/f$ filter in decade, and the poles and zeros are defined as

$$\begin{aligned} p_i &= -2\pi f_i \times 10^i, \quad i = 0, 1, ..., fdec - 1 \\ z_i &= p_i \times \sqrt{10}, \quad i = 0, 1, ..., fdec - 2. \end{aligned} \tag{4.13}$$

Here, $f_0$ is the lowest interested frequency of the filter, and the whole interested frequency band of the filter is from $f_0$ to $f_0 \times 10^{fdec}$. Defining the poles and zeros as in (4.13) will guarantee the frequency response of the transfer function in the interested frequency band has $1/f$ behavior. In our model, the input of the $1/f$ filter is a band-limited white noise with noise level of $1V/\sqrt{Hz}$. Hence, the level of the $1/f$ noise is only determined by the transfer function of the $1/f$ filter. Since the root mean square (RMS) value of the $1/f$ noise is usually defined as [13]

$$e_n = K\sqrt{\frac{1}{f}} \tag{4.14}$$

where $K$ is the value of $e_n$ at 1Hz, $\tilde{H}_{1/f}(s)$ is further modified by multiplying a gain $G$ in order that the amplitude of the frequency response is equal to $K$ at 1Hz. The gain $G$ is calculated by

$$G = \frac{K}{\tilde{H}_{1/f}(s)}|_{s=2\pi j} \tag{4.15}$$

and the modified transfer function $H_{1/f}(s)$ becomes

$$H_{1/f}(s) = G\tilde{H}_{1/f}(s). \tag{4.16}$$

As an example, the bode plot of the transfer function $H_{1/f}(s)$ for $f_0 = 10\mu$Hz, $fdec = 5$ and $K = 1$ is given in Fig. 4.8.

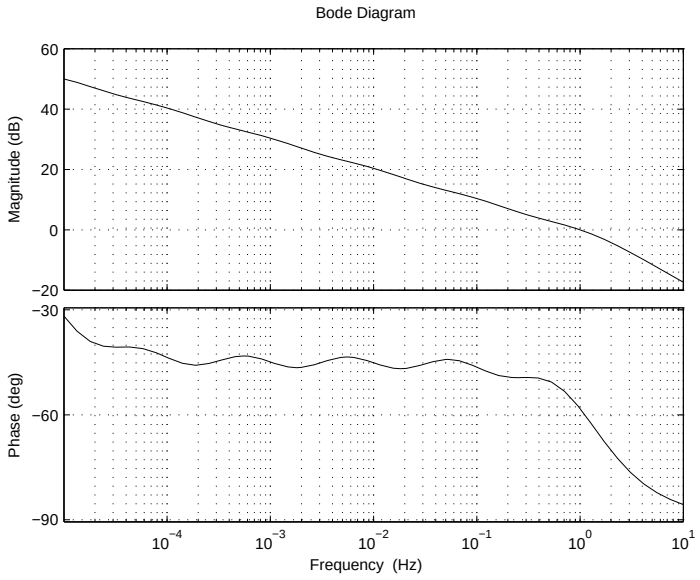


**Figure 4.8** Bode plot of the transfer function of the $1/f$ filter.

Chapter 5

# Exemplary Applications : Demos

In this chapter, several examples of the simulation using the Simscape and Simulink models for the IS FEE PFM hardware are demonstrated. These examples can be found in the "Demo" of the "Simscape Libaray" and "Simulink Library". The schematics and layouts of the IS FEE PFM sensing and actuation hardware can be found in [2].

## 5.1. IS FEE PFM Sensing Channel using Simscape Models

The IS FEE PFM sensing channel simulation using Simscape models is demonstrated in this section. In order to speed up the simulation, the simulation scheme is split into two parts, which are "transformer, TIAs and differential amplifier" and "bandpass filter and demodulator".

### 5.1.1. Transformer, TIAs and differential amplifier

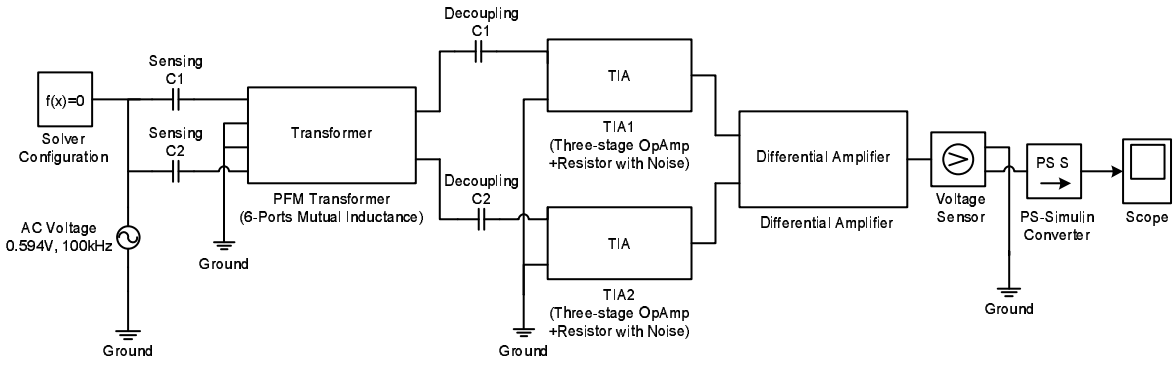


**Figure 5.1** Simscape PFM sensing part 1: Transformer, TIAs and Differential Amplifier.

The first part of the simulation scheme for the IS FEE PFM sensing using Simscape models is shown in Fig. 5.1. The models used in the simulation scheme are the "PFM Transformer

(6-Ports Mutual Inductance)", "TIA (Three-stage OpAmp + Resistor with Noise)", "Differential Amplifier" from the "Simscape Library" in the toolbox, the "AC Voltage Source", "Capacitor", "Voltage Sensor", "Ground", "PS-Simulink Converter", "Solver Configuration" from the "Foundation Library" and "Utilities" in Simscape, and the "Scope" from the "Commonly Used Blocks" in Simulink. Note that a "Solver Configuration" must be connected in the scheme in case Simscape models are used. "Voltage Sensor" is used to detect the voltage signal at the output of the differential amplifier, and then the voltage signal is converted to Simulink signal by the "PS-Simulink Converter" so that it can be observed by the "Scope".

The parameters for simulation configuration are defined as in Table 5.1, which can be defined in the simulation configuration panel by clicking "Simulation" $\rightarrow$ "Configuration Parameters ..." on the simulation scheme window.

| **Panels** | **Parameters** | **Values** |
|---|---|---|
| Simulation time | Start Time, Stop Time | 0.0, 0.001 |
| Solver options | Solver | ode15s (stiff/NDF) |
| | Relative tolerance | $10^{-6}$ |
| | Maximum order | 2 |
| Zero-crossing options | Algorithm | Adaptive |

**Table 5.1** Parameters for the simulation configuration.

The parameters of each blocks are defined similarly as in the PFM hardware, and the attenuated injection voltage is simulated by the "AC Voltage Source" with 0.594V amplitude and $100k$Hz frequency. The difference of the sensing capacitors C1 and C2 is converted to voltage signal by the transformer and TIAs, and this voltage signal is further amplified by the differential amplifier. The default values of the sensing capacitors C1 and C2 are $1.15+0.06$pF and $1.15-0.06$pF, respectively. With this setting, the theoretical output signal should be a $100k$Hz sin signal with 0.817V amplitude. In our simulation, the output signal at the "Scope" is a $100k$Hz sin signal with about 0.8V amplitude, as shown in Fig. 5.2.

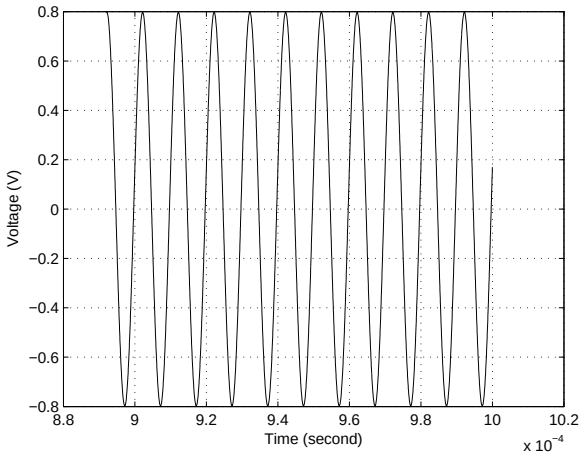


**Figure 5.2** Simulation results in scope for PFM sensing part 1.

### 5.1.2. Bandpass filter and demodulator

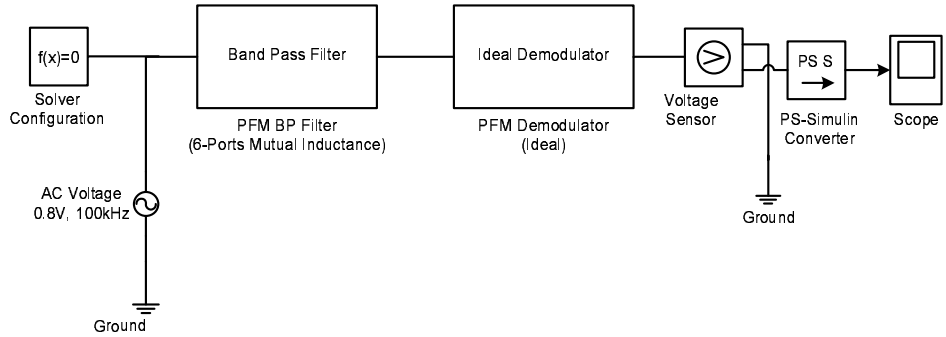


**Figure 5.3** Simscape PFM sensing part 2: Band Pass Filter and Demodulator.

The second part of the simulation scheme for the IS FEE PFM sensing using Simscape models is shown in Fig. 5.3. The models used in the simulation scheme are the "PFM BP Filter", "PFM Demodulator (Ideal)" from the "Simscape Library" in the toolbox, the "AC Voltage Source", "Voltage Sensor", "Ground", "PS-Simulink Converter", "Solver Configuration" from the "Foundation Library" and "Utilities" in Simscape, and the "Scope" from the "Commonly Used Blocks" in Simulink. The parameters for simulation configuration are defined similarly as in Table 5.1, except that the "Stop Time" is set as "0.02".

The parameters of each blocks are defined similarly as in the PFM hardware, and the input is simulated by the "AC Voltage Source" with 0.8V amplitude and $100k$Hz frequency, which is equal to the output of the differential amplifier in Section 5.1.1 when the difference between the sensing capacitor C1 and C2 is 0.12pF. The theoretical steady state output should be 2.32V and in our model, the steady state output at the "Scope" is 2.03V, as shown in Fig. 5.4.

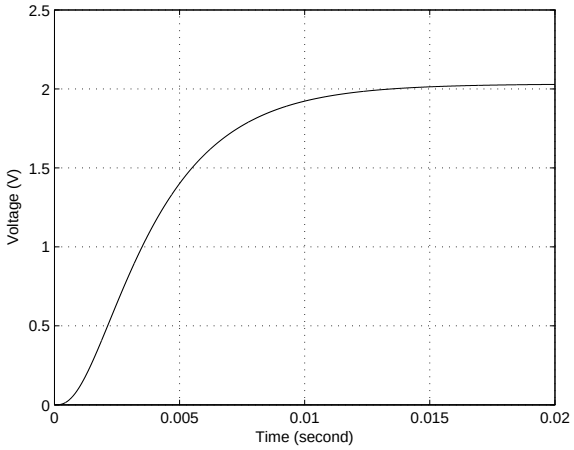


**Figure 5.4** Simulation results in scope for PFM sensing part 2.

## 5.2. IS FEE PFM Sensing Channel using Simulink Models

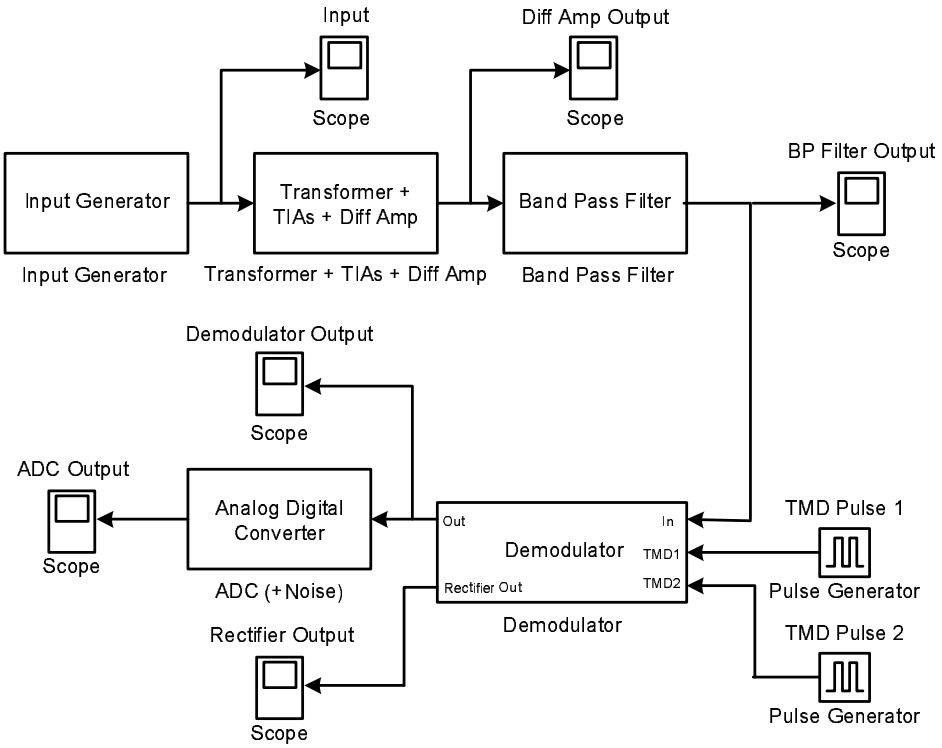


**Figure 5.5** Simulink PFM sening.

The simulation scheme for the IS FEE PFM sensing using Simulink models is shown in Fig. 5.5. The models used in the simulation scheme are the "Input Generator", "Transformer + TIAs + Diff Amp", "Band Pass Filter", "Demodulator", "ADC (+Noise)" from the "Simulink Library" in the toolbox, the "Pulse Generator" from the "Sources" and the "Scope" from the "Commonly Used Blocks" in Simulink. Since there is no Simscape model used in the scheme, the "Solver Configuration" block as in previous schemes is not needed. Also, the signal can be directly observed by the "Scope" without using the "Voltage Sensor" and "PS-Simulink Converter". The parameters for simulation configuration are defined similarly as in Table 5.1, except that the "Stop Time" is set as "0.03".

The sensing capacitors C1 and C2 in "Transformer + TIAs + Diff Amp" are defined as $1.15 + 0.06$pF and $1.15 - 0.06$pF, respectively, and other parameters are defined similarly as in the PFM hardware. The "TMD Pulse 1" and "TMD Pulse 2" signals are used to control the rectifier in the demodulator. The "TMD Pulse 2" is always half time cycle later than the "TMD Pulse 1", and the delay of "TMD Pulse 1" is adjusted to obtain fully positive signal at the "Rectifier Output" of the "Demodulator". The "TMD Pulse 1" and "TMD Pulse 2" signals in the simulation are defined in Table 5.2.

After simulation, the voltage outputs of the differential amplifier and band pass (BP) filter are shown in Figs. 5.6 and 5.7, respectively. The Voltage output of the demodulator and the output of the ADC are shown in Figs. 5.8 and 5.9, respectively.

| Pulse Signal | Amplitude | Period (secs) | Phase Delay (secs) |
|---|---|---|---|
| TMD Pulse 1 | 1 | $1/10^5$ | $164/360/10^5$ |
| TMD Pulse 2 | 1 | $1/10^5$ | $164/360/10^5 + 1/2/10^5$ |

**Table 5.2** Definition of the TMD pulses.

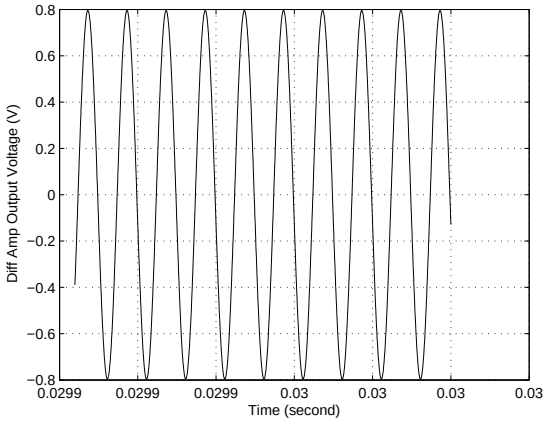


**Figure 5.6** Differential amplifier output: peak voltage is 0.7958V (theoretical 0.812V).

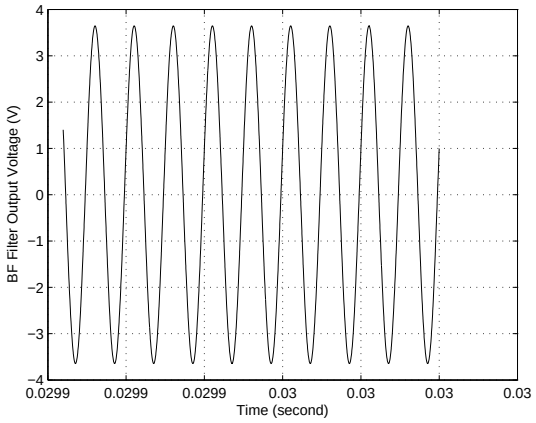


**Figure 5.7** Band pass filter output: peak voltage is 3.6448V (theoretical 3.64V).

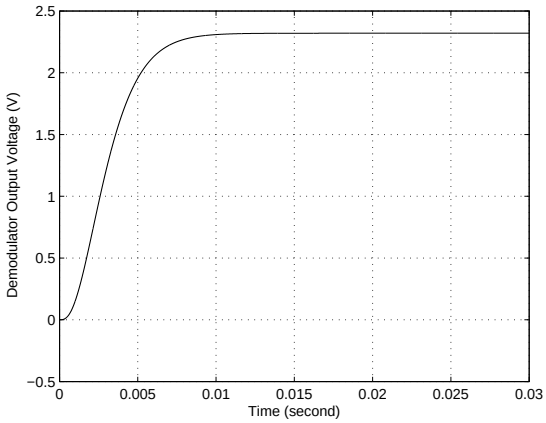


**Figure 5.8** Demodulator output: steady state voltage is 2.3199V (theoretical 2.32V).

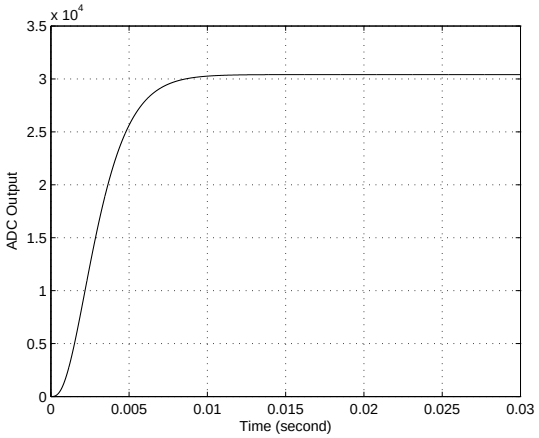


**Figure 5.9** ADC output: steady state output is 30408 (theoretical 30408).

## 5.3. Sigma-Delta Loop Simulation using Simulink Models

### 5.3.1. IS FEE actuation: sigma-delta loop (Version 1.0)

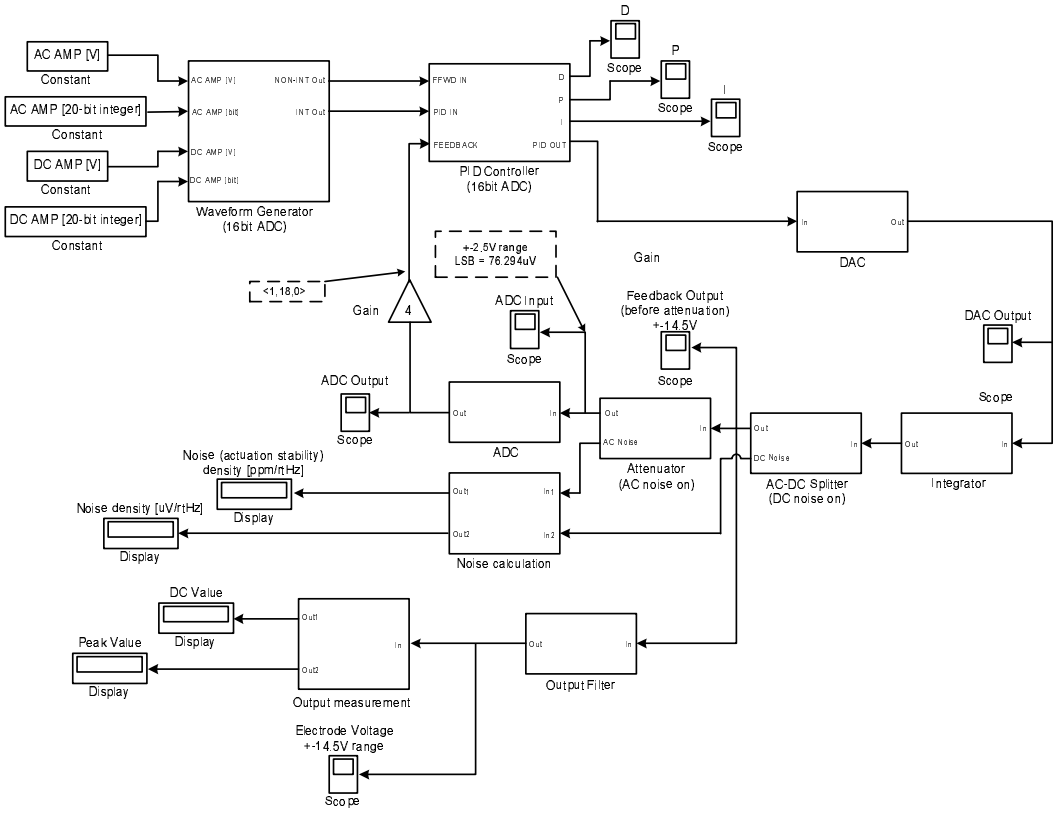


**Figure 5.10** Simulink PFM actuation sigma-delta loop (Version 1.0).

The simulation scheme (version 1.0) for the IS FEE PFM actuation sigma-delta loop using Simulink models is shown in Fig. 5.10. The models used in the simulation scheme are the "Waveform Generator (16bit ADC)", "PID Controller (16bit ADC)", "DAC", "Integrator", "AC-DC Splitter", "Output Filter", "Attenuator", "ADC" from the "Simulink Library" in the toolbox, and the "Constant", "Gain", "Scope", "Display" from the "Commonly Used Blocks" and "Sinks" in Simulink. The definition of the inputs for the "Waveform generator (16bit ADC)" are given in Table 5.3. The parameters for simulation configuration are defined similarly as in Table 5.1, except that the "Stop Time" is set as "3/80". Note that the "Stop Time" should be equal to or greater than this value, in order to obtain correct estimate values at the output of the "Output measurement" block.

In this simulation, "16 bits" command is used in the "Waveform Generator (16bit ADC)" and "PID Controller (16bit ADC)". The "High PID Precision" switches in these two blocks are turned off. The ideal ADC model is used and the DAC noise is switched off. In order to simulate the noise, the AC noise in the "Attenuator" and DC noise in the "AC-DC Splitter" should be switched on.

The output signal formats of some blocks are given in the form of $< S, N, D >$, where $S$ denotes the number of bits for the sign, $N$ denotes the total number of bits for the signal, and

| Inputs [Unit] | Range | Output Data Type | LSB |
|---|---|---|---|
| AC AMP [V] | $0 \sim 10V$ | unsigned | - |
| AC AMP [bit] | $0 \sim 1048575$ | unsigned | $9.537\mu V$ |
| DC AMP [V] | $-5V \sim 5V$ | double | - |
| DC AMP [bit] | $-524287 \sim 524287$ | double | $9.537\mu V$ |

**Table 5.3** Definition of the inputs for "Waveform Generator".

$D$ denotes the number of bits for the decimal. The root mean square (RMS) values of the AC and DC noise are calculated by the "Noise calculation" block and can be observed by the "Display". The output of the "AC-DC Splitter" is filtered by the "Output Filter" to obtain the electrode voltage. The DC and peak value of the electrode voltage is also measured by the "Output measurement" block.

As mentioned in Section 3.2.1, the PFM hardware uses 16 bits as the waveform amplitude, and the 20 bits waveform amplitude is only provided as an option to investigate benefit of better resolution. Also, the waveform generator input in bits, i.e., "AC AMP [bit]" and "DC AMP [bit]", is based on 20-bit resolution. However, the model chooses the right number of bits according to the option of amplitude command bits "AMP CMD". For simulation of the PFM hardware, the "Amplitude Command Bits" in the "Waveform Generator" should be set as "16".

### 5.3.2. IS FEE actuation: sigma-delta loop (Version 2.0)

The simulation scheme (version 2.0) for the IS FEE PFM actuation sigma-delta loop using Simulink models is shown in Fig. 5.11. The models used in the simulation scheme are the "Waveform Generator (16bit ADC)", "PID Controller (16bit ADC)", "DAC", "Integrator", "AC-DC Splitter", "Output Filter", "Attenuator", "ADC (+Noise)" from the "Simulink Library" in the toolbox, and the "Transfer Fcn", "Constant", "Gain", "Scope", "Display" from the "Commonly Used Blocks" and "Sinks" in Simulink.

Compared to the simulation scheme (version 1.0), the AC noise in the "Attenuator" is turned off, and the AC noise is simulated in the "ADC (+Noise)" model. The parameters setup for the "ADC (+Noise)" model is given in Table 5.4. The DC noise in the "AC-DC Splitter" is still switched on. The purpose of this change is to make the simulation more close to the real hardware. Note that $Var_{ref}$ in the "ADC (+Noise)" model simulates the $3ppm/\sqrt{Hz}$ voltage reference stability.

The output of the AC-DC splitter circuit before the LP filter with corner frequency $3.9k$Hz is filtered by a HP filter with corner frequency $1k$Hz, in order to measurement the wide band DC noise with removed possible DC level. The output of the electrode is further filtered by a LP filter with corner frequency 5Hz, in order to simulate the measurement using digital multimeter (DMM) in the real hardware measurement.

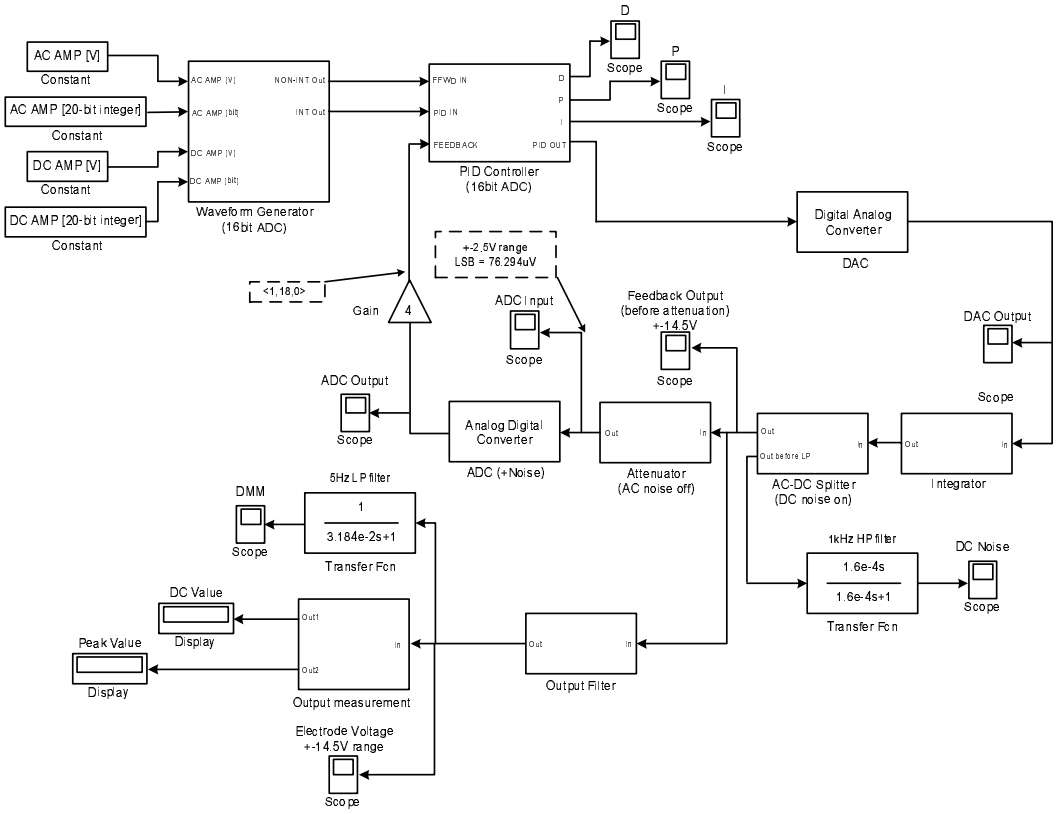


**Figure 5.11** Simulink PFM actuation sigma-delta loop (Version 2.0).

| **Parameters (Unit)** | **Values** |
|---|---|
| $N$ (Bits) | 16 |
| $V_{ref}$ (V) | 2.5 |
| $SINAD$ (dB) | 86 |
| $Var_{ref}$ $(V^2)$ | $(3 \times 10^{-6} \times 2.5 \times \sqrt{12000})^2$ |
| $T_s$ (s) | $1/(96 \times 10^3)$ |
| Neg_Out | Yes |
| Noise Switch On | Yes |

**Table 5.4** Parameters setup for "ADC (+Noise)".

### 5.3.3. IS FEE actuation: measurement investigation (Version 1.0)

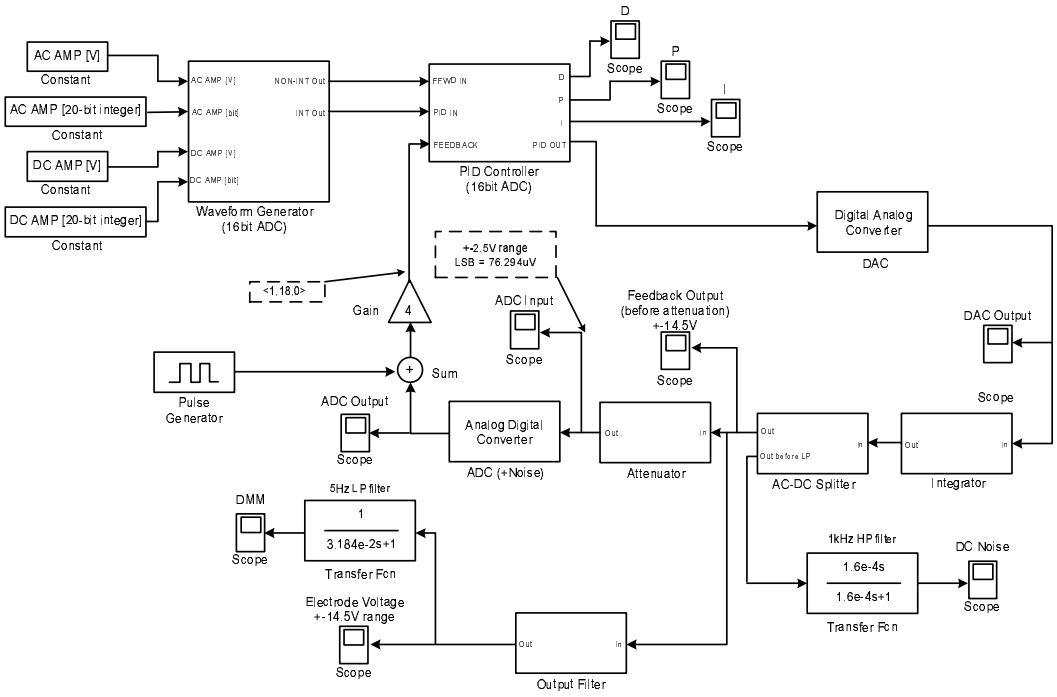


**Figure 5.12** Simulink PFM actuation measurement investigation (Version 1.0).

The simulation scheme (version 1.0) for the actuation stability test of IS FEE PFM hardware using Simulink models is shown in Fig. 5.12. The models used in the simulation scheme are the "Waveform Generator (16bit ADC)", "PID Controller (16bit ADC)", "DAC", "Integrator", "AC-DC Splitter", "Output Filter", "Attenuator", "ADC (+Noise)" from the "Simulink Library" in the toolbox, and the "Transfer Fcn", "Constant", "Gain", "Pulse Generator", "Sum", "Scope", "Display" from the "Commonly Used Blocks" and "Sinks" in Simulink.

Since unexpected voltage jumps are observed at the electrode using DMM in the real actuation stability test, pulse generators are used in the scheme in order to reproduce the jump and hence to investigate the sources of the jumps. Here, a pulse generator is used to generate 1 LSB error at the output of the ADC to simulate an ADC glitch error that occurs every $2ms$ and lasts for $0.2ms$, which is approximately 20 ADC readings. The other pulse generator is used in the attenuator after the attenuation gain to simulate the attenuator error. The parameters of the pulse generators are defined in Table 5.5.

| **Pulse Generator** | **Amplitude** | **Period** [s] | **Width** [% of Period] | **Delay** [s] |
|---|---|---|---|---|
| Output of ADC | $-1$ LSB | 0.002 | 10 | 0.7 |
| Attenuator | $-8 \times 10^{-6}$ V | 1 | 10 | 1 |

**Table 5.5** Definition of the pulse generator.

The simulation of DMM measurement with ADC error is shown in Fig. 5.13. The pulse

generator in the attenuator is switched off. A jump is expected to be observed starting at 0.7 second at the electrode and the zoom in of Fig. 5.13 around 0.7 second with voltage range $4.5V \pm 150\mu V$is shown in Fig. 5.14. We can see that a jump with voltage about $50\mu V$ is observed after 0.7 second. The jump is 1/10th of the ADC LSB size scaled to the electrode output, i.e. 10% of 444$\mu$V, and since the error glitch is repetitive, an output offset is observed. Note that this jump simulation has a multiplicative effect as in the hardware.

The simulation of DMM measurement with attenuator offset error is shown in Fig. 5.15. The pulse generator at the output of the ADC is switched off. A jump is expected to be observed starting at 1 second at the electrode and the zoom in of Fig. 5.15 around 1 second with voltage range $4.5V \pm 150\mu V$is shown in Fig. 5.16. We can see that a jump with voltage about $50\mu V$ occurs after 1 second. The simulated jump of 8$\mu$V at the output of the attenuator will be equivalent to the electrode output of $8\mu \times 14.5/2.5 = 46.4\mu$V. Note that this jump simulation has an additive effect, while the hardware shows a multiplicative effect according to the gain fluctuation.

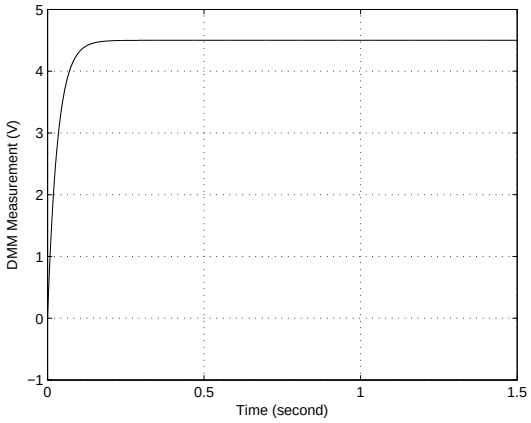


**Figure 5.13** ADC error simulation.

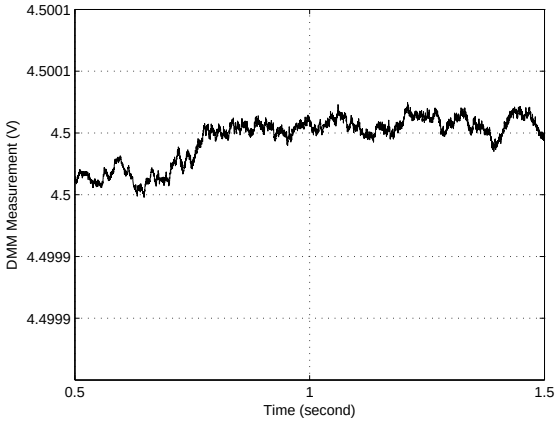


**Figure 5.14** ADC error simulation zoom in.

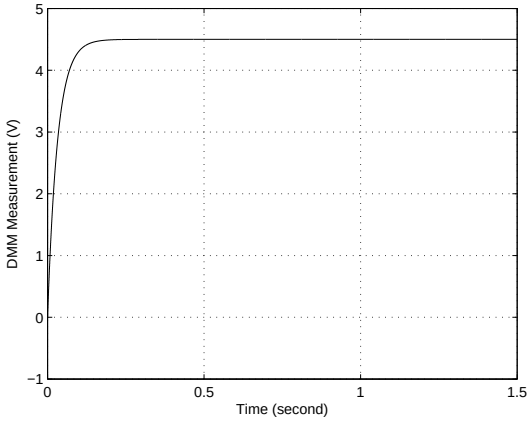


**Figure 5.15** Attenuator error simulation.

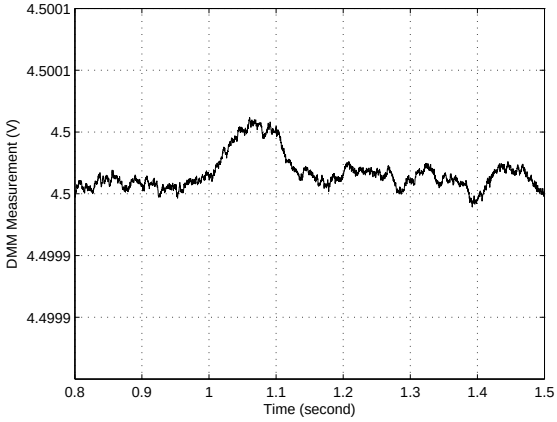


**Figure 5.16** Attenuator error simulation zoom in.

### 5.3.4. GRS FEE actuation: sigma-delta loop

The first simulation scheme for the GRS FEE actuation sigma-delta loop using Simulink models is similar as Fig. 5.11. However, "20 bits" command is used in the "Waveform Generator (16bit ADC)" and "PID Controller (16bit ADC)" instead of "16 bits" command using in the IS FEE actuation sigma-delta loop simulation. Also, the "High PID Precision" switches in these two blocks can be turned on or off for investigation.

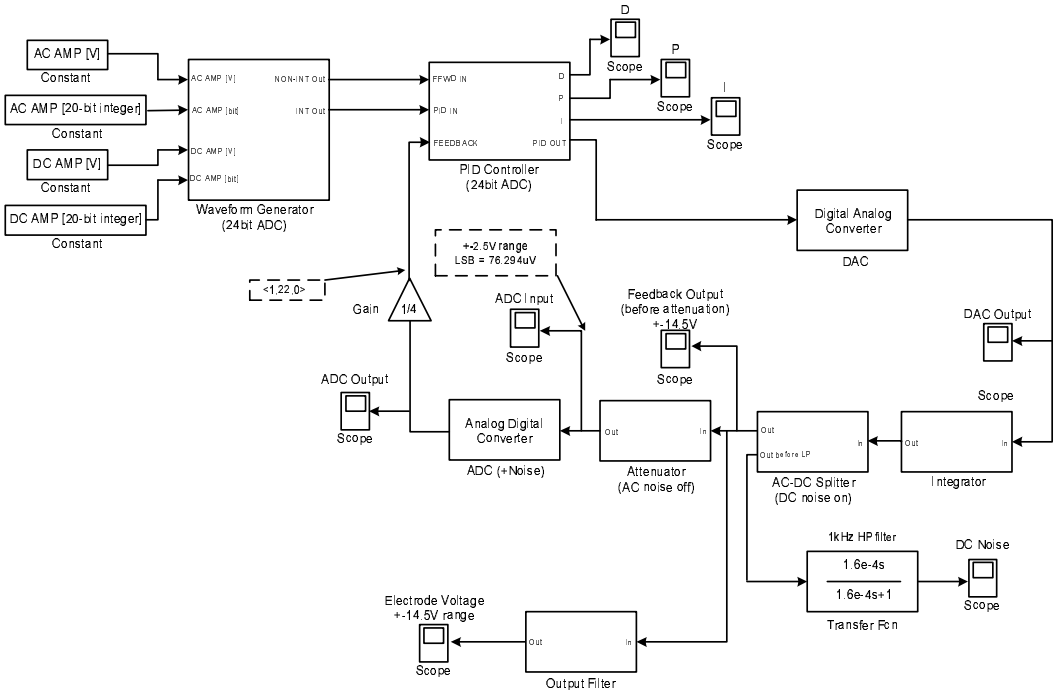


**Figure 5.17** Simulink GRS FEE actuation sigma-delta loop.

The second simulation scheme for the GRS FEE actuation sigma-delta loop using Simulink models is given in Fig. 5.17. In this simulation scheme, "20 bits" command is used, "Waveform Generator (24bit ADC)" and "PID Controller (24bit ADC)" are used in order to improve the performance.

The detail of the above mentioned simulation and results can be found in Appendix A.3 and [14].

## 5.4. IS FEE PFM Hardware using Simplified Models

### 5.4.1. PFM sensing: M-File S-Function models

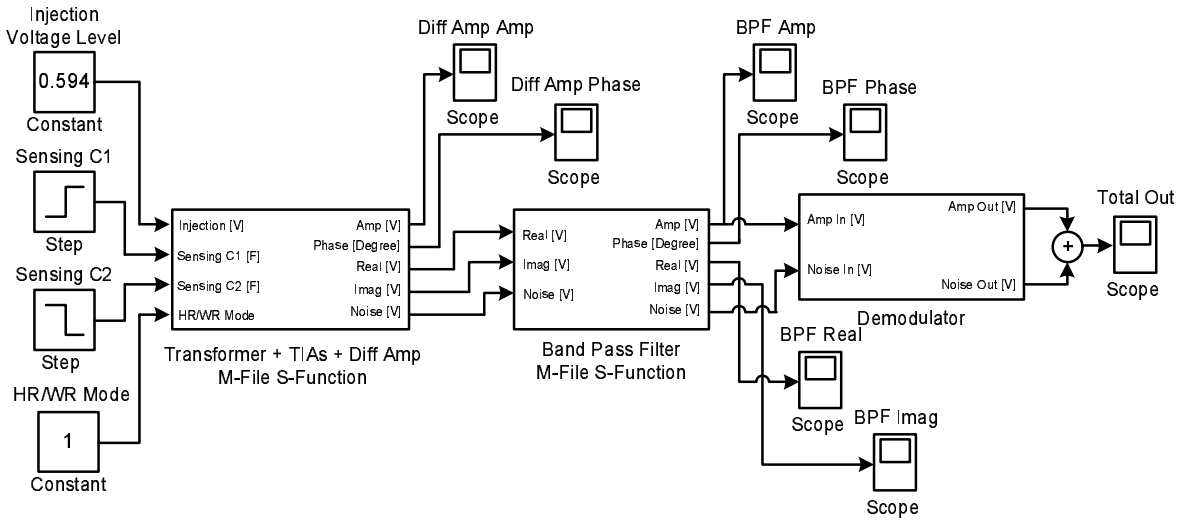


**Figure 5.18** Simplified PFM sensing using M-File S-Function models

The simulation scheme for the IS FEE PFM sensing using M-File S-Function models is shown in Fig. 5.18. The models used in the simulation scheme are the "Transformer + TIAs + Diff Amp (M-File S-Function)", "Band Pass Filter (M-File S-Function)", "Demodulator" from the "Simplified Library" in the toolbox, the "Constant", "Step" from the "Sources" and the "Sum", "Scope" from the "Commonly Used Blocks" in Simulink. The parameters for simulation configuration are defined similarly as in Table 5.1, except that the "Stop Time" is set as "10". The sensing capacitors C1 and C2 are modeled using "Step" blocks with values changing from 1.15pF to $1.15 + 0.06$pF and $1.15 - 0.06$pF, respectively. The zoom in simulation result in the "Total Out" scope is shown in Fig. 5.19.

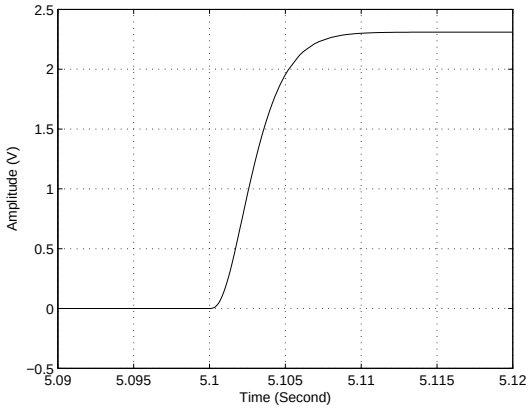


**Figure 5.19** Simulation results in the scope "Total Out" (zoom in).

### 5.4.2. PFM sensing: C S-Function models

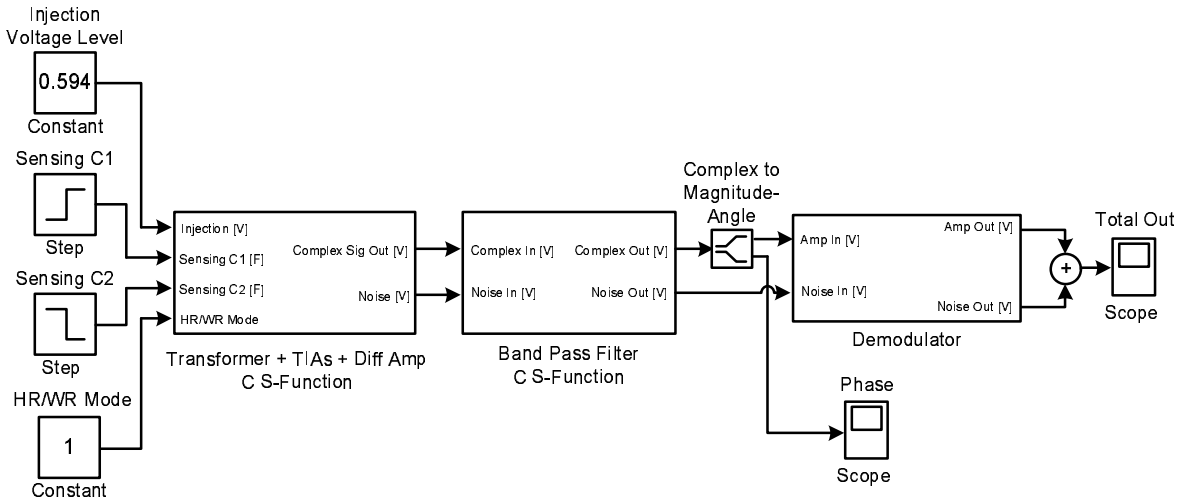


**Figure 5.20** Simplified PFM sensing using C S-Function models

The simulation scheme for the IS FEE PFM sensing using C S-Function models is shown in Fig. 5.20. The models used in the simulation scheme are the "Transformer + TIAs + Diff Amp (C S-Function)", "Band Pass Filter (C S-Function)", "Demodulator" from the "Simplified Library" in the toolbox, the "Constant", "Step" from the "Sources", the "Complex to Magnitude and Angle" from the "Math Operations" and the "Sum", "Scope" from the "Commonly Used Blocks" in Simulink. The parameters for simulation configuration are defined similarly as in Table 5.1, except that the "Stop Time" is set as "10". The sensing capacitors C1 and C2 are modeled using "Step" blocks with values changing from 1.15pF to $1.15 + 0.06$pF and $1.15 - 0.06$pF, respectively. The zoom in simulation result in the "Total Out" scope is shown in Fig. 5.21.

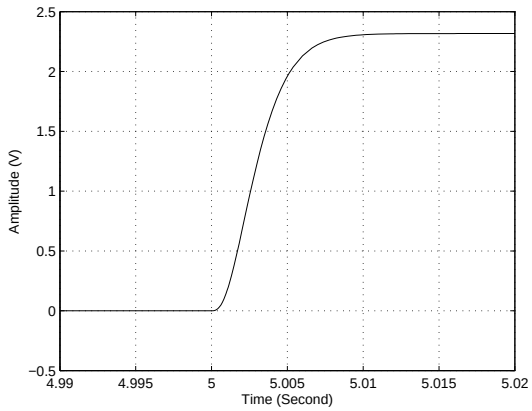


**Figure 5.21** Simulation results in the scope "Total Out" (zoom in).

### 5.4.3. PFM actuation to sensing cross talk

The simulation scheme for the IS FEE PFM sensing using M-File S-Function model or C S-Function models is similar as in Fig. 5.18 or Fig. 5.20. The sensing capacitors C1 and C2 are modeled using "Step" blocks with values changing from 1.15pF to $1.15 + 0.06$pF and $1.15 - 0.06$pF at the 5th second of the simulation, respectively. The actuation input Vact1 is also modeled using "Step" blocks with values changing from 0 to 2V at the 8th second of the simulation, and the actuation input Vact2 keeps zero. The simulation results on the scope "Total Out" using the M-File S-Function models are shown in Fig. 5.22 and Fig. 5.23. The simulation results on the scope "Total Out" using the C S-Function models are shown in Fig. 5.24 and Fig. 5.25. From the simulation results, we can see that the cross talk happens when the actuation inputs are active.

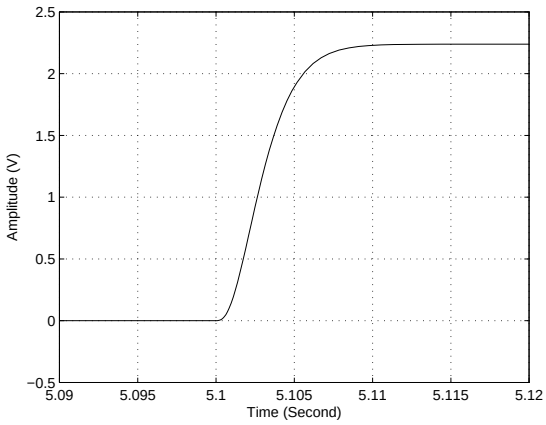


**Figure 5.22** Zoom in around 5.1s.

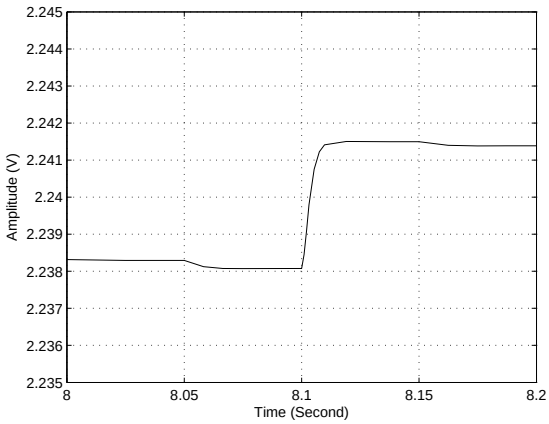


**Figure 5.23** Zoom in around 8.1s.

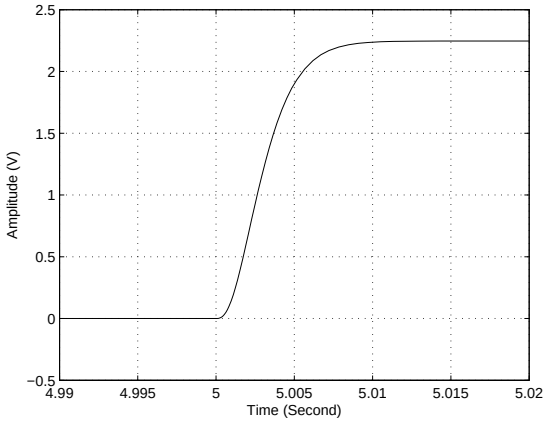


**Figure 5.24** Zoom in around 5s.

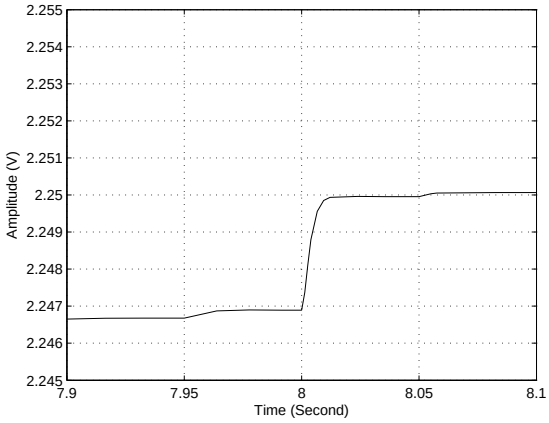


**Figure 5.25** Zoom in around 8s.

Chapter A

# Appendix

## A.1. Resonance Tuning Capacitance

As mentioned in Section 3.1.1, the transformer can be equivalent to a voltage source $V_{oc}$ in series with an impedance $Z_{eq}$, and the impedance $Z_{eq}$ is defined as

$$Z'_{eq} = \frac{j\omega(1-j\delta)L_3}{-\omega^2(1-j\delta)[M_{13}r_1(C_1+C_{p1})+M_{23}r_2(C_2+C_{p2})]+1}. \tag{A.1}$$

Here, $s = j\omega$, $\delta = 1/Q$, $Q$ is the quality factor, $M_{13}$ and $M_{23}$ are the mutual inductances, $r_1$ and $r_2$ are defined as

$$r_1 = \frac{C_{a1}}{C_{a1}+C_{p1}+C_1}, \quad r_2 = \frac{C_{a2}}{C_{a2}+C_{p2}+C_2} \tag{A.2}$$

where $C_{a1}$ and $C_{a2}$ are the actuation capacitances, $C_1$ and $C_2$ are the sensing capacitances, $C_{p1}$ and $C_{p2}$ are the resonance tuning capacitances. By defining

$$B = M_{13}r_1(C_1+C_{p1}) + M_{23}r_2(C_2+C_{p2}) \tag{A.3}$$

we have

$$Z'_{eq} = \frac{\omega\delta L_3 + j\omega L_3}{1-\omega^2 B + j\omega^2\delta B} = \omega L_3 \frac{\delta + j}{1-\omega^2 B + j\omega^2\delta B}. \tag{A.4}$$

Multiplying the numerator and denominator of (A.4) with $1-\omega^2 B - j\omega^2\delta B$ and replacing $\delta$ by $1/Q$ gives

$$\begin{aligned} Z'_{eq} &= \omega L_3 \frac{(\delta+j)(1-\omega^2 B - j\omega^2\delta B)}{(1-\omega^2 B)^2 + (\omega^2\delta B)^2} = \omega L_3 \frac{\delta + j(1-\omega^2 B - \omega^2\delta^2 B)}{(1-\omega^2)^2 + (\omega^2\delta B)^2} \\ &= \omega L_3 \frac{Q + j[Q^2(1-\omega^2 B) - \omega^2 B]}{Q^2(1-\omega^2)^2 + (\omega^2 B)^2}. \end{aligned} \tag{A.5}$$

At the resonance frequency $f_0$, $Z'_{eq}$ looks like a resistance and the reactive component of $Z'_{eq}$ is equal to zero, that is

$$Q^2(1-\omega_0^2 B) - \omega_0^2 B = 0 \tag{A.6}$$

where $\omega_0 = 2\pi f_0$. Hence, the resonance frequency $f_0$ can be written as

$$f_0 = \frac{Q}{\sqrt{1+Q^2}} \frac{1}{2\pi\sqrt{B}} = \frac{Q}{\sqrt{1+Q^2}} \frac{1}{2\pi\sqrt{M_{13} r_1 (C_1 + C_{p1}) + M_{23} r_2 (C_2 + C_{p2})}}. \tag{A.7}$$

Assuming $M_{13} = M_{23} = M$, $C_{a1} = C_{a2} = C_a$, $C_{p1} = C_{p2} = C_p$, $C_1 = C_2 = C_0$ and $Q \gg 1$, $f_0$ can be simplified to

$$f_0 \approx \frac{1}{2\pi\sqrt{M \frac{C_a}{C_a + C_p + C_0} (2C_0 + 2C_p)}}. \tag{A.8}$$

Knowing the resonance frequency $f_0$, the resonance tuning capacitance $C_p$ can be calculated by

$$C_p = \frac{C_a + C_0 - 2M\omega_0^2 C_a C_0}{2M\omega_0^2 C_a - 1}. \tag{A.9}$$

In our model, by defining $Q = 200 \gg 1$, $f_0 = 100k\text{Hz}$, $M = 4.2m\text{H}$, $C_a = 10n\text{F}$ and $C_0 = 1.15p\text{F}$, the calaculated resonance tuning capacitance $C_p$ is approximately $310p\text{F}$.

## A.2. PSDs of the Noise Sources at the TIAs Output

### A.2.1. Transformer impedance noise

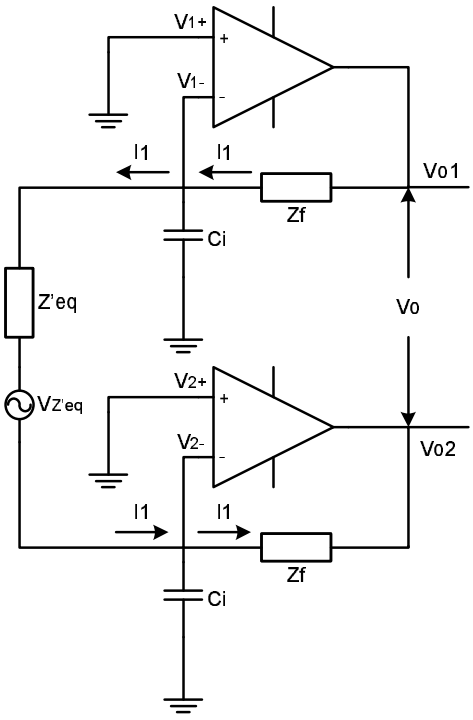


**Figure A.1** The TIAs output: the transformer impedance noise .

The schematic of analyzing the TIAs output of the transformer impedance noise is shown in Fig. A.1. The OpAmps in the circuit are considered to be ideal, $V_{Z'eq}$ is the transformer impedance noise voltage source, $C_i$ is the TIA input capacitance - JFET input capacitance, $Z'_{eq}$ and $Z_f$ are the transformer equivalent impedance and the feedback impedance of the TIA, respectively, as defined in Section 3.1.1.

Since the OpAmps are ideal, we have

$$\begin{aligned} V_{1+} &= V_{1-} = 0 \\ V_{2+} &= V_{2-} = 0. \end{aligned} \tag{A.10}$$

Hence, there is no current flow through both $C_i$, otherwise $V_{1-}$ will be nonzero. $I_1$ in the circuit can be written as

$$I_1 = \frac{V_{Z'eq} - V_{1-}}{Z'_{eq}} = \frac{V_{Z'eq}}{Z'_{eq}}. \tag{A.11}$$

Consequently, the potential $V_{o1}$ and $V_{o2}$ can be written as

$$\begin{aligned} V_{o1} &= V_{1-} + I_1 Z_f = I_1 Z_f \\ V_{o2} &= V_{2-} - I_1 Z_f = -I_1 Z_f. \end{aligned} \tag{A.12}$$

Therefore, the output voltage $V_o$ is (*cf.* (A.11) and (A.12))

$$V_o = V_{o1} - V_{o2} = 2I_1 Z_f = \frac{2Z_f}{Z'_{eq}} V_{Z'eq}. \tag{A.13}$$

### A.2.2. Voltage noise source

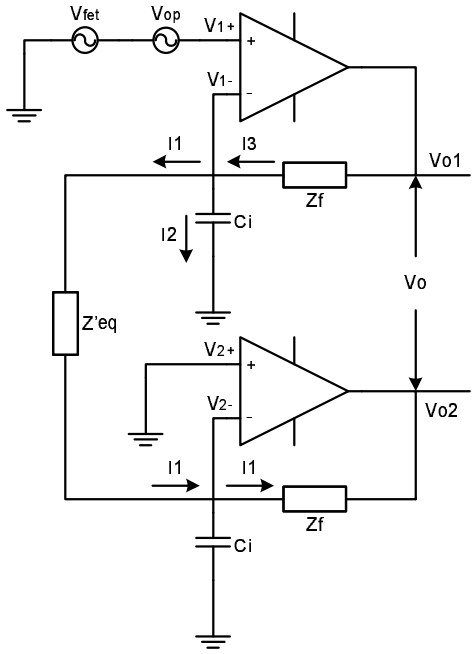


**Figure A.2** The TIAs output: voltage noise sources at one OpAmp + input.

The schematic of analyzing the TIAs output with voltage noise sources at one OpAmp positive input is shown in Fig. A.2. $V_{fet}$ and $V_{op}$ are the JFET and OpAmp voltage noise sources, respectively.

Since the OpAmps are ideal, we have

$$\begin{aligned} V_{1-} &= V_{1+} = V_{fet} + V_{op} \\ V_{2-} &= V_{2+} = 0. \end{aligned} \tag{A.14}$$

Hence, the currents $I_1$ and $I_2$ can be written as

$$\begin{aligned} I_1 &= \frac{V_{1-} - V_{2-}}{Z'_{eq}} = \frac{V_{1-}}{Z'_{eq}} \\ I_2 &= \frac{V_{1-}}{1/sC_i}. \end{aligned} \tag{A.15}$$

Since $I_3$ is equal to $I_1 + I_2$, $V_{o1}$ becomes

$$V_{o1} = V_{1-} + I_3 Z_f = V_{1-} + (I_1 + I_2) Z_f. \tag{A.16}$$

Also, $V_{o2}$ is calculated as

$$V_{o2} = V_{2-} - I_1 Z_f = -I_1 Z_f. \tag{A.17}$$

Therefore, the output voltage $V_o$ is (*cf.* (A.14) to (A.17))

$$\begin{aligned} V_o &= V_{o1} - V_{o2} \\ &= V_{1-} + (2I_1 + I_2)Z_f \\ &= (1 + \frac{2Z_f}{Z'_{eq}} + \frac{Z_f}{1/sC_i})V_{1-} \\ &= (1 + \frac{2Z_f}{Z'_{eq}} + \frac{Z_f}{1/sC_i})(V_{fet} + V_{op}). \end{aligned} \tag{A.18}$$

Equivalent analysis can be done for the voltage noise sources at the other OpAmp positive input.

The schematic of analyzing the TIAs output with voltage noise sources at one OpAmp negative input is shown in Fig. A.3. Note that normally the OpAmp voltage noise source is only considered at the positive input for the sake of simplicity, here we consider the voltage noise sources at both positive and negative inputs in order to obtain more accurate model.

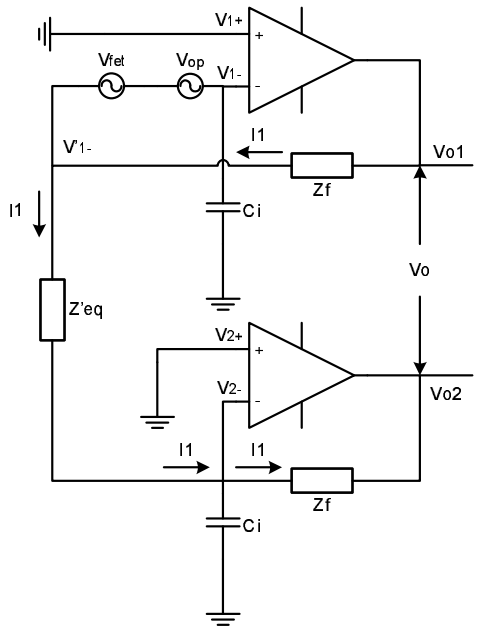


**Figure A.3** The TIAs output: voltage noise sources at one OpAmp - input.

Since the OpAmps are ideal, we have

$$\begin{aligned} V_{1+} = V_{1-} = 0 \\ V_{2+} = V_{2-} = 0. \end{aligned} \tag{A.19}$$

Hence the potential $V'_{1-}$ is

$$V'_{1-} = V_{1-} + V_{fet} + V_{op} = V_{fet} + V_{op} \tag{A.20}$$

and the current $I_1$ can be written as

$$I_1 = \frac{V'_{1-} - V_{2-}}{Z'_{eq}} = \frac{V'_{1-}}{Z'_{eq}}. \tag{A.21}$$

Consequently, the potential $V_{o1}$ and $V_{o2}$ can be written as

$$\begin{aligned} V_{o1} &= V'_{1-} + I_1 Z_f \\ V_{o2} &= V_{2-} - I_1 Z_f = -I_1 Z_f. \end{aligned} \tag{A.22}$$

Therefore, the output voltage $V_o$ is (*cf.* (A.20) to (A.22))

$$V_o = V_{o1} - V_{o2} = V'_{1-} + 2I_1 Z_f = (1 + \frac{2Z_f}{Z'_{eq}})V'_{1-} = (1 + \frac{2Z_f}{Z'_{eq}})(V_{fet} + V_{op}). \tag{A.23}$$

Equivalent analysis can be done for the voltage noise sources at the other OpAmp negative input.

### A.2.3. Current noise source

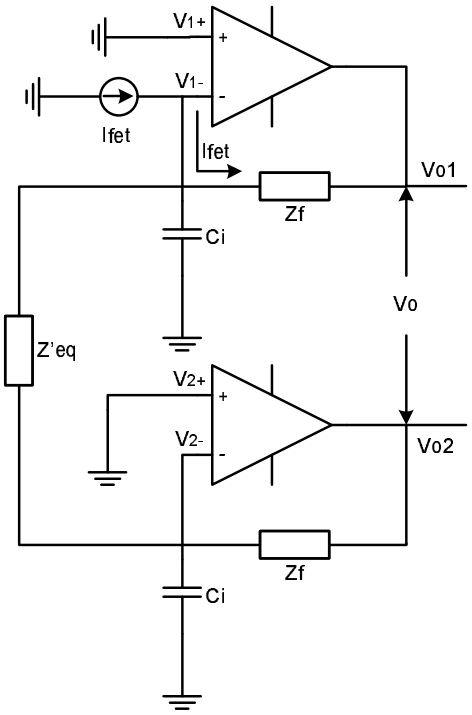


**Figure A.4** The TIAs output: current noise sources at one TIA input.

The schematic of analyzing the TIAs output of one TIA input current noise source is shown in Fig. A.4. Since the OpAmps are ideal, we have

$$\begin{aligned} V_{1+} &= V_{1-} = 0 \\ V_{2+} &= V_{2-} = 0. \end{aligned} \tag{A.24}$$

The noise input current $I_{fet}$ can not flow through $C_i$ or $Z'_{eq}$, otherwise $V_{1-}$ or $V_{2-}$ will be nonzero. Therefore, the output voltage $V_o$ is simply

$$V_o = I_{fet} Z_f. \tag{A.25}$$

## A.3. Waveform Generator and PID Controller

The entire actuation circuit is the sigma-delta loop, containing digital part and analog part. The digital part is implemented on FPGA, including waveform generator and proportional-integral-derivative (PID) controller. The analog part contains D/A converter (DAC), integrator, AC-DC splitter, attenuator and the feedback ADC.

Since all commands are implemented as binary vectors in FPGA, $< S, N, D >$ is used to represent the fix-point data format for real number value of the command, where $S$, $N$ and $D$ denote the number of bits for the sign, total data length and decimal data length, respectively.

### A.3.1. 16-bit ADC and 16-bit CMD

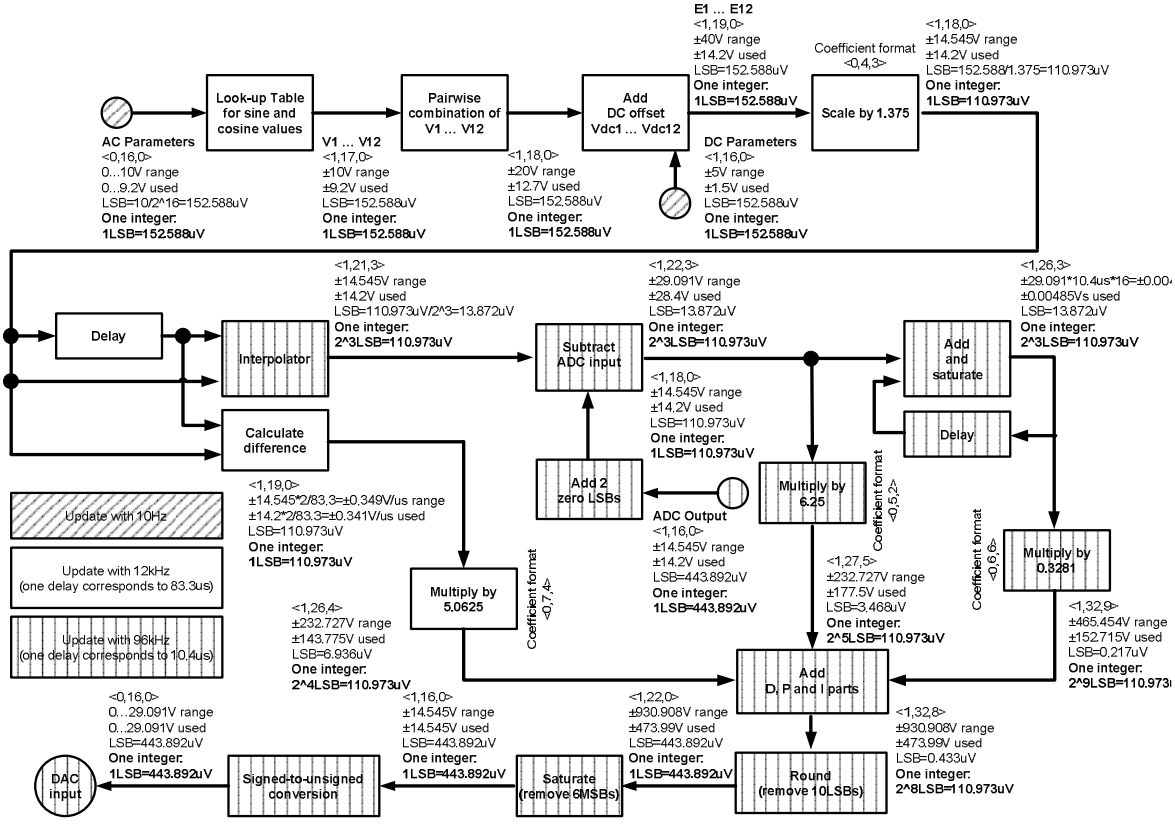


**Figure A.5** Waveform generator for 16-bit ADC and 16-bit CMD.

A detailed description of the digital part of the IS FEE actuation circuit, i.e. the waveform generator and PID controller implemented on FPGA, is given in Fig. A.5. The LSB value of the command (of the last decimal) at the output of each block is given. The equivalent number of LSBs for one integer is also given.

The input AC and DC parameter commands are 24 bits. However, 4 (zero) MSBs and 4 (non-zero) LSBs are cut in the existing IS FEE design for the HR mode and thus the AC and DC parameter commands become with 16-bit resolution.

The "scale K" operation is defined as multiplying the input command by the scale factor $K$ without modifying the used range of the real value that the command represents. This operation is used to change the LSB value by the factor $1/K$. For example, in the "scale by 1.375" block, the LSB value of the electrode voltage "$E_1E_{12}$" is 152.588$\mu$V and the used range of the real value is $\pm$14.2V. After the "scale by 1.375" operation, the LSB value reduces to $152.588/1.375 = 110.973\mu$V and the used range of the real value stays the same.

The "multiply by K" operation is defined as multiplying the input command by the scale factor K and modifying the used range of the real value that the command represents by the factor K. For example, the output of the "Subtract ADC input" block has data format of $< 1, 22, 3 >$ and the used range of the real value is $\pm$28.4V. Via the "multiply by 6.25" operation with coefficient data format of $< 0, 5, 2 >$, the command is increased by 6.25 times and the data format becomes $< 1, 27, 5 >$, and the used range of the real value is increased to $\pm$177.5V. Since 2 extra bits are added to present the decimal value, the LSB value reduces from 13.872$\mu$V to $13.872/22 = 3.468\mu$V.

In addition, the "round (remove K LSBs)" operation removes $K$ LSBs from the command and in consequence magnifies the LSB value by the factor $2K$. The "Saturate (remove K MSBs)" operation removes $K$ MSBs from the command without changing the LSB value.

The LSB value and the range of the DAC input in Fig. A.5 is the value with respect to the actuation output, i.e. the electrode voltage. Note that the "Signed-to-unsigned conversion" operation is used to convert the signed command into the equivalent unsigned command, since the DAC input should have the data format of $< 0, 16, 0 >$.

### A.3.2. 16-bit ADC and 20-bit CMD

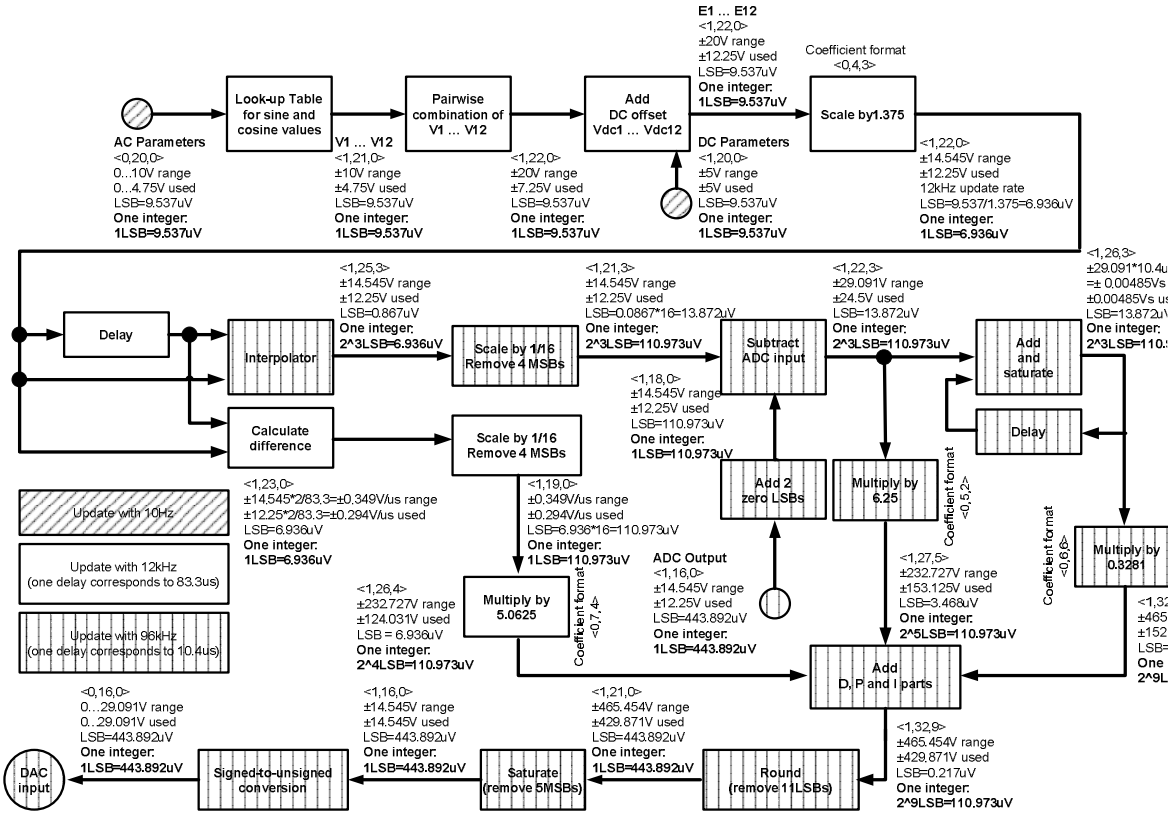


**Figure A.6** Waveform generator for 16-bit ADC and 20-bit CMD with low PID precision.

In the GRS FEE, the AC and DC parameter commands shall be 20 bits, i.e. cutting only 4 (zero) MSBs from the input commands and thus not losing the resolution provided by the DFACS. For the 20-bit AC and DC parameter commands, the digital part of the actuation circuit is modified and shown in Fig. A.6. The additional 4 bits, compared to the IS FEE, improve the interpolator amplitude level setting resolution to 6.936$\mu$V. Finally, the removal of these additional 4 bits is done before the PID controller to maintain the same design as in IS FEE with LSB of 110.973$\mu$V. Therefore, the first proposed GRS FEE actuation circuit architecture is based on using 20-bit AC and DC parameter commands with 16-bit ADC.

A further investigation of the first proposed GRS FEE actuation circuit architecture is also based on 20-bit AC and DC parameters commands with 16-bit ADC, but with high PID controller precision as shown in Fig. A.7.

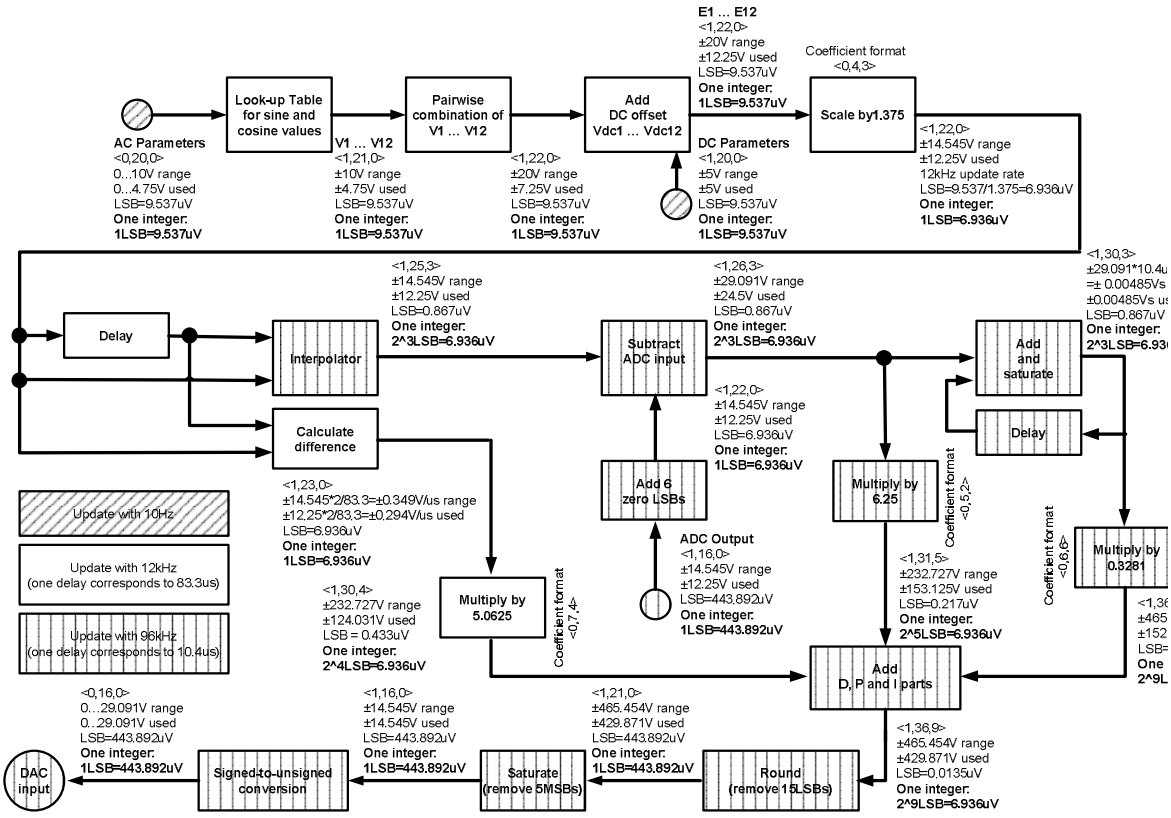


**Figure A.7** Waveform generator for 16-bit ADC and 20-bit CMD with high PID precision.

### A.3.3. 24-bit ADC and 20-bit CMD

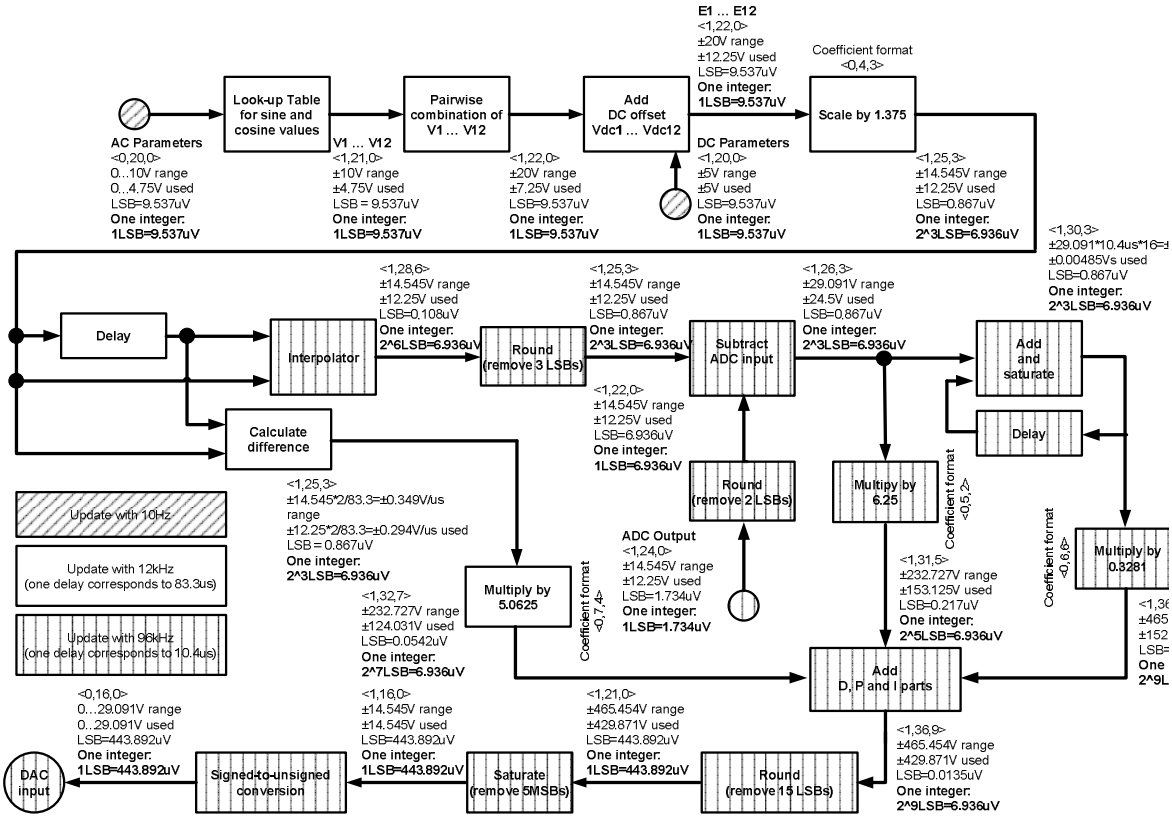


**Figure A.8** Waveform generator for 24-bit ADC and 20-bit CMD.

Since the ADS1278-HT, 24-bit ADC is currently under radiation testing, the digital part of the actuation circuit can be further modified by the use of this part, as shown in Fig. A.8. Thus, the second proposed GRS FEE actuation circuit architecture is based on using 20-bit AC and DC parameter commands with the 24-bit feedback ADC.

Chapter B

# Change Record

| Version | Date | Change Description | Section |
|---|---|---|---|
| 1.0 | 03.2010 | first version | all |
| 1.1 | 23.04.2010 | correct and update the ADC model | Section 3.1.4 |
| | | update the Simulink simulation scheme "PFM Actuation (Version 1.0)" | Section 5.3 |
| 1.2 | 27.04.2010 | modify the "Integrator" model | Section 3.2.4 |
| | | add Simulink model "DAC (+Noise)" | Section 3.2.3 |
| | | add Simulink model "AC-DC splitter (without noise)" | Section 3.2.5 |
| | | add Simulink model "Attenuator (without noise)" | Section 3.2.6 |
| | | add Simulink simulation scheme "PFM Actuation (Version 2.0)" | Section 5.3 |
| | | update the structure of the Simulink library | Section 1.2 |
| | | update the user guide | Section 1.3 |
| | 04.05.2010 | update the structure of the Simulink library | Section 1.2 |
| 1.3 | 04.05.2010 | add Simulink model "Attenuator (with pulse)" | Section 3.2.6 |
| | | correct typos in the figures | Section 5.1 5.2 |
| | | add Simulink simulation scheme "PFM Actuation Measurement Investigation (Version 1.0)" | Section 5.3 |
| | | update the structure of the Simulink library | Section 1.2 |
| | | update the user guide | Section 1.3 |
| 1.4 | 25.05.2010 | correct and update | all |
| 1.5 | 09.06.2010 | modify the noise model in the Simulink model "Transformer+TIAs+Diff Amp" | Section 3.1.1 |
| | | add the analysis of the noise model | Appendix A.2 |
| 2.0 | 25.06.2010 | change the default value of the sampling time | Section 3.1.1, 3.1.5 |
| | 08.2010 | add Simplified library | Chapter 4 |
| 2.1 | 09.2010 | correct the transfer function derivation | Section 3.1.1 |
| | | add cross talk models | Section 4.1.1 |

| Version | Date | Change Description | Section |
|---|---|---|---|
| 2.5 | 04.2011 | update the Simulink and Simplified sensing models, based on the cross talk investigation | Section 3.1, 4.1 |
| | | regulate the Simulink actuation models (merge, delete, etc.) | Section 3.2 |
| | | add Simulink models for GRS FEE, i.e. waveform generator and PID controller | Section 3.2.1, 3.2.2 |
| | | update the introduction and simulation scheme, i.e. cross talk investigation, GRS FEE actuation | Section 1, 5 |
| | | update the appendix, i.e. GRS FEE actuation | Section A.3 |
| 2.6 | 12. 2011 | modify the introduction and other typos | all |

**Table B.1** Change record of the toolbox and user manual.

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